MODEL 371

Source Locking
Autohet Microwave Counter

Operating & Service Manual

Serial Prefix/CCN Group beginning:

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SECTION

CERTIFICATION

EIP Incorporated certifies that this instrument was thoroughly inspected and tested, and found to be in conformance with the specifications noted herein at time of shipment from factory.

WARRANTY

EIP Incorporated warrants this counter to be free from defects in material and workmanship for one year from the date of delivery. Damage due to accident, abuse, or improper signal level, is not covered by the warranty. Removal, defacement, or alteration, of any serial or inspection label, marking, or seal, may void the warranty. EIP Incorporated will repair or replace at its option, any components of this counter which prove to be defective during the warranty period, provided the entire counter is returned PREPAID to EIP or its authorized service facility. In-warranty counters will be returned freight prepaid; out-of-warranty units will be returned freight COLLECT. No other warranty other than the above warranty is expressed or implied. EIP Incorporated and Danalab Incorporated, are not liable for consequential damages.

ASSISTANCE

For assistance, contact the EIP representative in your area, or EIP Incorporated.

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GENERAL INFORMATION & SPECIFICATIONS

1-1. DESCRIPTION

1-2. The EIP 371 Source Locking Autohet Microwave Counter automatically measures the frequency of any CW signal within the range of 20 Hz to 18.0 GHz. This frequency range is covered in three bands: 20 Hz to 300 MHz, 100 MHz to 850 MHz, and 825 MHz to 18 GHz.

1-3. Measurements in Band I (20 Hz to 300 MHz) are made with a 300 MHz direct electronic counter. Band II (100 MHz to 850 MHz) uses a prescaler to divide the input signal by a factor of four into the frequency range of the 300 MHz direct counter. Band III (850 MHz to 18.0 GHz) measurements are made by heterodyning the input frequency with an automatically selected harmonic of an internal 200 MHz comb generator, producing a difference frequency which falls within the range of the 300 MHz direct counter. The inaccuracy of the indicated reading by the counter, is directly related to the quality of the time base oscillator over the entire operating range of the counter (see Sections 1 and 6).

1-4. The display on the 371 Counter provides a direct readout of the measured frequency over the entire operating range of the counter. The 371 Counter also includes automatic suppression of leading zeros, except during a no signal input condition.

1-5. The frequency readout of the 371 Counter is displayed in a fixed position format that is conveniently sectionalized in GHz, MHz, kHz, and Hz. Four gate times: 1 ms, 10 ms, 100 ms, and 1 second, are automatically selected depending upon the setting of the RESOLUTION switch.

1-6. For applications where less resolution is required, pushbutton display blanking (RESOLUTION) is provided to simplify the readout.

1-7. To assure trouble-free performance, the EIP 371 Counter is completely solid-state. For ease of repair and maintenance, the major portion of the counter circuitry is contained on plug-in printed circuit boards or in easily removed modules. Special test points allow monitoring of critical circuit functions.

1-8. INSTRUMENT IDENTIFICATION

1-9. The 371 Counter is identified by two number sets: the Model and Configuration Control Number (e.g. 371-CCN 1201), and a specific Serial Number (e.g. 12345). BOTH SETS OF NUMBERS should be noted in any correspondence or parts orders regarding the counter.

1-10. SPECIFICATIONS

1-11. EIP 371 Source Locking Microwave Counter specifications are given in Table 1-1.

NOTICE

GENERAL:

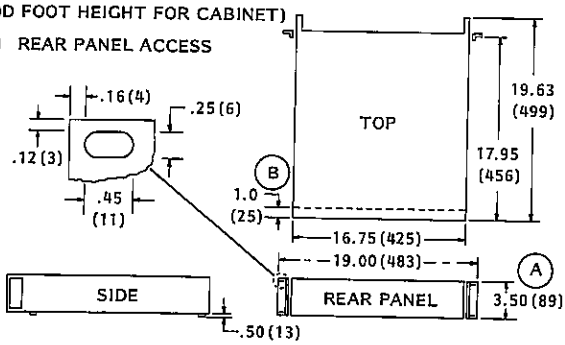
Frequency Range:	20 Hz - 18.0 GHz.
Accuracy:	±1 count ± time base accuracy.
Resolution:	1 Hz to 1 MHz in decade steps.
Gate Time:	1 sec (1 Hz), 0.1 s (10 Hz), 10 ms (100 Hz), 1 ms (1 kHz, 10 kHz, 100 kHz, 1 MHz). Band II gate times are expanded by four.
Sample Rate:	Controls time between measurements. Variable, 100 ms - 1 s (typ).
Display:	11 digit light-emitting diode (LED); sectionalized to read: GHz, MHz, kHz, and Hz.
Operation:	Completely automatic after setting input selector.
Acquisition Time:	In Band III, comb line acquisition requires 10 ms/GHz plus 50 ms (nominal). Once locked, readings can be taken at rate determined by Sample Rate control and selected gate time.
Operating Temp:	0° to +50°C.
Power:	115/230 Vac ±10%, 50-60 Hz, 90 watts (nominal).
Weight:	Shipping: 30.0 lbs (13.6 kg); Net: 25.5 lbs (11.6 kg).
Access. Furnished:	Detachable power cord, 8 ft (241 cm) long, with plug; Operating & Service manual; extender card.
Access. Available:	Rack Mount Kit: P/N: 2010008. Carrying Case: P/N: 5700001. Calibration Kit: P/N: 2000005.

DIMENSIONS (mm)

(A) E.I.A. RACK HEIGHT

(ADD FOOT HEIGHT FOR CABINET)

(B) REAR PANEL ACCESS



All specifications subject to change at manufacturers discretion.

CONTROLS:

See Figures 3-1 and 3-2, and Tables 3-1 and 3-2.

TIME BASE (STANDARD):

Crystal Frequency:	10 MHz.
Stability:	
Aging Rate:	$< \lvert 3 \times 10^{-7} \rvert$/month.
Short Term:	$< 1 \times 10^{-9}$ rms for one second averaging time.
Temperature:	$< \lvert 2 \times 10^{-6} \rvert$ between 0° to +50°C.
Line Variation:	±10% line voltage change results in a frequency shift of $< \lvert 1 \times 10^{-7} \rvert$.
Warm-up Time:	None.
Output Freq:	10 MHz, square-wave, 1 V p-p minimum into 50 ohms.
Ext. Time Base:	Requires 10 MHz, 1 V p-p minimum into 300 ohms.

SIGNAL INPUTS:

BAND IA:

Frequency Range:	20 Hz - 135 MHz
Min. Sensitivity:	25 mV rms
Input Impedance:	1 megohm/20 pf
Maximum Input:	120 V rms (Note 1)
Max. Input without Damage:	150 V rms (Note 1)
Coupling:	AC
Connector:	BNC female

Note 1: Above 1 kHz maximum input decreases at 6 dB/octave rate to 3.0 V.

BAND IB:

Frequency Range:	10 MHz - 300 MHz
Min. Sensitivity:	-20 dBm (22 mV rms)
Input Impedance:	50 ohms nominal
Maximum Input:	+10 dBm (0.7 V rms)
Max. Input without Damage:	+27 dBm (5.0 V rms)
Coupling:	AC
Connector:	BNC female

TABLE 1-1. SPECIFICATIONS - 371 COUNTER

SIGNAL INPUTS (CONTINUED):

BAND II:

Frequency Range:	10 MHz - 850 MHz
Min. Sensitivity:	100 MHz - 150 MHz: -15 dBm (40 mV rms). 150 MHz - 850 MHz: -20 dBm (22 mV rms).
Maximum Input:	+10 dBm (0.7 V rms)
Max. Input without Damage:	+27 dBm (5.0 V rms)
Input Impedance:	50 ohms nominal
Coupling:	AC
Connector:	BNC female

BAND III:

Frequency Range:	825 MHz - 18.0 GHz.
Min. Sensitivity:	825 MHz - 1.1 GHz: -25 dBm (12 mV rms), 1.1 GHz - 12.4 GHz: -30 dBm (7 mV rms), 12.4 GHz - 18.0 GHz: -25 dBm (12 mV rms).
Maximum Input:	+7 dBm, +20 dBm typ.
Max. Input without Damage:	+33 dBm (2 watts).
Input Impedance :	50 ohms nominal.
Coupling:	AC.
Connector:	Type N Precision female.
VSWR:	2.5 : 1 typical.
FM Tolerance:	40 MHz p-p, worst case, for modulation rates from DC to 10 MHz.
YIG Preset:	
Selection:	Front panel keyboard input; indicated on 6-digit LED display.
Settability:	Set ≥ 400 MHz below lowest frequency to be measured. Sweep begins at preset and measures only frequencies ≥ 400 MHz above preset frequency.
Operation:	Preset desired frequency on keyboard in MHz (or GHz) at 200 MHz increments. Press PRESET button.

SOURCE LOCKING SPECIFICATIONS:

Freq. Coverage:	10 MHz - 18.0 GHz.
Resolution:	100 kHz (400 kHz in Band II).
Long Term Stability:	Equal to counter time base osc.
Minimum Lock Level:	Equal to counter sensitivity.
Lock Time:	0.1 - 3 s; dependent on source.
Accuracy:	Equal to counter.
Capture Range:	± 20 MHz min; ± 50 MHz typical unless limited by source characteristics or output current capability.
Bandwidth and Polarity:	Fully automatic selection.
Output Drive Capability:	± 10 V into 5 Kohm min, or ± 40 mA into 10 ohms max.
Output Connector:	Rear panel BNC female.
Residual FM Reduction:	See graph below for typical response.
Required Source Input Characteristics:	
Bandwidth:	4 kHz min for specified performance.
Modulation Sensitivity:	Voltage input (R_{in} > 5 Kohm): 2 to 200 MHz/V. Current input (R_{in} < 10 ohms): 0.1 to 10 MHz/mA.

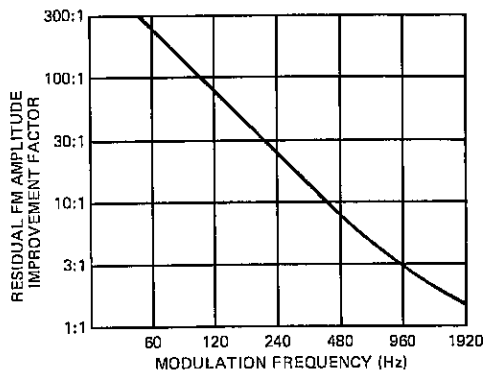


TABLE 1-1 (Continued). SPECIFICATIONS - 371 COUNTER

SECTION 2

INSTALLATION

2-1. UNPACKING

2-2. The EIP 371 Source Locking Autohet Microwave Counter arrives ready for operation. Carefully inspect the shipping carton before opening for any evidence of visible or concealed damage. If any seems apparent, ask that the shipper's agent be present when the instrument is unpacked.

2-3. Remove the packing carton and supports, being careful not to scar or damage the instrument. Make a complete visual inspection of the counter, checking for any damage or missing components. Check that all switches and controls operate mechanically. Report any damage to EIP immediately.

2-4. INSTALLATION

2-5. There are no special installation instructions for the 371 Microwave Counter. The unit is a self-contained bench or rack mounted instrument, which only requires connection to a standard, single-phase, 115/230 V, 50-60 Hz power line for operation. CAUTION: Check current rating of counter fuse and setting of rear panel 115/230 Vac slide switch before applying power to counter.

2-6. INCOMING OPERATIONAL CHECK

2-7. The following procedure outlines an operational check of the counter which may be conducted without special tools, signal generators, or test equipment. The internal TIME BASE CLOCK is used as the input signal to the 300 MHz counter, therefore it cannot check the operation of the Band II prescaler or the Band III comb generator.

a. Turn counter POWER switch off. Check fuse rating and setting of 115/230 switch (on rear panel).
b. Connect counter power cord to a source of 115 or 230 V, 50-60 Hz, single-phase power. The ground terminal on the power cord plug should connect to a reliable earth ground.
c. Press POWER switch (on front panel) to turn counter on. The counter display should light, and the internal cooling fan should operate.
d. Place the rear panel TIME BASE INT/EXT switch in the INT position.
e. Partially depress any one of the RESOLUTION switches and release it so no switch remains in the depressed position. All digits in the 11-digit display should indicate "0" (zero).
f. Depress the TEST switch on the front panel. The display should indicate 10 000 000 (10 MHz). Note that the three leading zeros are blanked (not lit).
g. Blank the 1 Hz digit by pressing the right hand RESOLUTION switch.
h. Depress the TEST button again. The display should still indicate 10 MHz, but with the final "0" blanked. Also note a decrease in the gate time evidenced by the shorter on-time of the GATE light.
i. Test each RESOLUTION switch in turn, starting with the 1 Hz digit. Note that the digit immediately above that switch, and all digits to the right of that switch, are blanked.
j. Unblank all display digits (see "e." above for procedure).
k. With no signal input, the entire display* should show all zeros in all bands.
l. Depress both the TEST and RESET switches simultaneously. All display digits* should show "8" (all segments of each display lighted).
m. Set counter to Band IB (10 MHz - 300 MHz range). Program the auxiliary display (through keyboard entry) to read "10.0" MHz. Press LOCK button. LOCK indicator should light for 2-3 seconds then go out.
n. Set counter to Band III (850 MHz - 18 GHz range). Program the auxiliary display (as above) to read "10". Press PRESET button. Auxiliary display readout should now read "10000.0 (10 GHz), and PRESET indicator should light. Press CLR (Clear) button.
o. This completes the counter confidence check. All CW signals within the frequency range of the counter may be counter and locked. Refer to Section 1 for proper signal levels. If the counter fails to perform as described above, refer to Section 5.

* Except those on the Auxiliary Display panel.

SECTION 3

OPERATION

3-1. INTRODUCTION

3-2. The 371 incorporates two microwave instruments in one package: a wide range frequency counter, and a source locking device (lockbox) operating in conjunction with a frequency source. Essentially all of the operations are completely automatic, however attention should be paid to this section to note the procedures required for optimum performance of the instrument.

3-3. CONTROLS, INDICATORS AND CONNECTORS

3-4. Front panel controls, indicators and connectors are shown in Figure 3-1 and described in Table 3-1. Rear panel controls and connectors are shown in Figure 3-2 and described in Table 3-2.

3-5. NUMERICAL DISPLAY BRIGHTNESS ADJUSTMENT

3-6. Apparent brightness of the 11-digit light-emitting-diode (LED) visual display may be varied by adjustment of A103R20. (R20 is located near the top front of PC board A103, and is accessible by removing the top cover of the counter.) Adjust R20 clockwise to increase display brightness, or counter-clockwise to reduce brightness.

3-7. COUNTER OPERATION

a. Turn counter power on. Counter will automatically select Band III (825 MHz - 18 GHz).

b. Pressing the BAND SELECT button once sets the counter to Band IA (20 Hz - 135 MHz). Pressing the button repeatedly will successively set the counter to Bands IB, II, III, IA, etc.

c. Select the desired operating band. Apply a signal to the appropriate input connector. If the signal is within counter specifications, the counter will automatically display the input frequency. See CAUTION notice regarding input level.

d. Select the desired sample rate and resolution (see Table 3-1).

CAUTION

DO NOT APPLY A SIGNAL EXCEEDING THE MAXIMUM INPUT SPECIFICATION TO ANY INPUT. EXTENSIVE DAMAGE NOT COVERED BY THE WARRANTY WILL OCCUR, WHETHER COUNTER IS TURNED ON OR OFF, OR APPEARS TO BE INOPERATIVE.

3-8. LOCKBOX OPERATION

a. Set up counter and signal source as described in paragraph 3-7.

b. Tune source within capture range of desired frequency (see Table 1-1, Specifications).

c. Keyboard desired frequency into Auxiliary Display (see Table 3-1). When the LOCK button is pressed, the Auxiliary Display will go out, and the LOCK indicator will glow brightly (during determination of loop polarity and gain). When the loop locks, the Auxiliary Display relights, while the LOCK indicator returns to its normal intensity. If the 371 cannot secure a lock, the LOCK indicator goes out, and the Auxiliary Display shows the programmed frequency. (If this situation occurs, compare the programmed frequency with the displayed input frequency. Check for an error in programming, input signal level or frequency, capture range limits exceeded, etc.)

d. When locking to a Band II input frequency (100 - 850 MHz), the signal source can be locked only at 400 kHz increments (due to Prescaler operation). To avoid the necessity of having the operator compute the valid frequencies, the counter automatically "rounds down" the input to the nearest frequency divisible by four. In Band II then, when the Auxiliary Display reappears after pressing the LOCK button, the frequency programmed may be different from that entered, whether or not a lock was obtained.

3-9. PRESET OPERATION

3-10. The YIG Preset function is available only in Band III (825 MHz - 18 GHz), and serves to initiate the counter's signal search at a higher start frequency than zero. This function serves to minimize signal acquisition time, and allows the Converter to ignore spurious or undesired signals below the one to be measured.

3-11. Keyboard the desired preset frequency into the Auxiliary Display and press the PRESET button. The counter will automatically justify the data entry to a multiple of 200 MHz, and begin its search at the frequency indicated. For example: If 12.5 GHz is entered via the keyboard, and the PRESET button is pressed, the Auxiliary Display will show 12400.0 MHz, the PRESET indicator will light, and the search will begin at 12.4 GHz. NOTE: Because data entries below 100 MHz are invalid, the 371 interprets entries between 1 - 99 MHz as 1 - 99 *GHz*.

(Continued on Page 3-4)

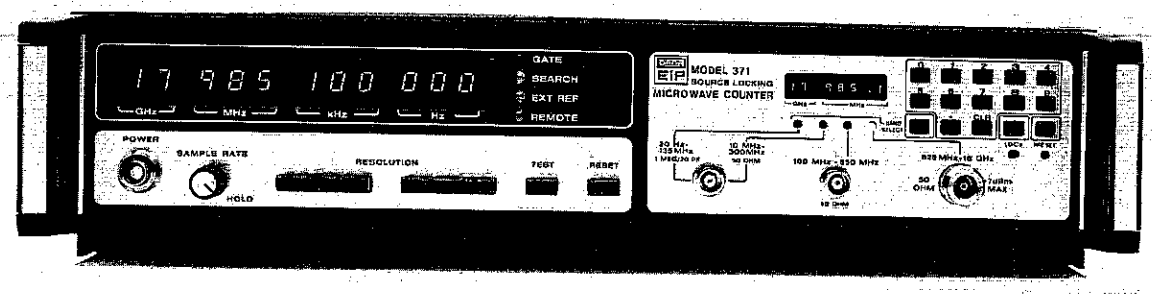


FIGURE 3-1. FRONT PANEL CONTROLS, INDICATORS AND CONNECTORS

POWER On/Off Switch

Turns counter power on and off.

SAMPLE RATE/HOLD Control

Varies time between measurements from 1/10 to 10 seconds (nominal) per reading. (Gate time is added to sample time, thus minimum reading time for 1 Hz resolution is 1.1 sec.) Last reading retained indefinitely in HOLD.

RESOLUTION Switches

Six pushbutton switches allow blanking (turning off) of the six least significant digits in the visual display. Each switch blanks the digit above and all digits to the right of that switch. Four gate times appropriate to the required resolution are also selected. 1 Hz resolution is achieved by partially depressing and releasing one of the switches (this action releases all the switches).

TEST Switch▲

Pressing the TEST switch places the counter in the self-test mode, with the test signal derived from the internal 10 MHz Time Base. Proper display is: 10 000 000 (10 MHz).

RESET Switch▲

This switch manually over-rides all controls, resets the counter and converter, and initiates a new reading.

Visual Display (left side of panel)

The 11-digit LED (light-emitting-diode) display provides a direct numerical readout of the input frequency. The display is sectionalized into GHz, MHz, kHz, and Hz.

GATE Indicator

Lights when signal gate is open.

SEARCH Indicator

Provides visual indication that the Converter is *not* locked to an input signal.

EXT REF Indicator

Lights when counter is set to EXT REF (External Time Base Reference) via rear panel switch. CAUTION: Lamp does not indicate level of external reference signal.

REMOTE Indicator

Used only with Option 07 (Remote Programming) and 17 (General Purpose Interface Bus). See Option section.

Keyboard Switches

Switches 0-9 enter numerical data into auxiliary display. Pressing the BAND SELECT pushbutton sets the counter to the next higher band, then repeats from the lowest band (e.g. II, III, IA, IB, II, etc.). Decimal point button designates the end of MHz data entry; following digit entered in .1 MHz position. LOCK button tells counter to lock the source being controlled to the frequency shown on the auxiliary display. PRESET button sets Band III start frequency to that shown on auxiliary display.

Auxiliary Display (right side of counter)

Six digit LED display indicates frequencies set by LOCK and PRESET buttons.

BAND SELECT Indicators

Indicate the operating range of the counter as determined by the keyboard BAND SELECT pushbutton switch.

LOCK and PRESET Indicators

Refer to Lockbox operation paragraphs in this section for a description of various indicator conditions.

Band I and Band II Input Connectors

Type BNC female. For measurements in the 20 Hz - 135 MHz (Band IA), 10 MHz - 300 MHz (Band IB), and 100 MHz - 850 MHz (Band II) frequency ranges.

Band III Input Connector

Type N precision female. For measurements in the 825 MHz - 18 GHz frequency range. See CAUTION notice in Section 3 regarding maximum input levels.

▲VISUAL DISPLAY TEST: Pressing *both* TEST and RESET switches simultaneously, will cause all numeric display digits to show the numeral "8" (all segments lighted).

TABLE 3-1. FRONT PANEL CONTROLS, INDICATORS AND CONNECTORS

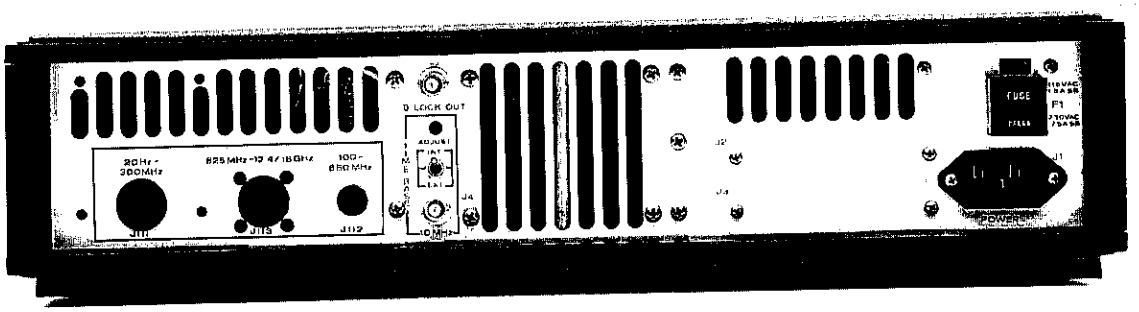


FIGURE 3-2. REAR PANEL CONTROLS AND CONNECTORS

Rear Panel Inputs

Openings allow simple modification for rear inputs.

ϕ LOCK OUT Connector

Provides output control signal to external frequency source when locking source to keyboard programmed frequency.

TIME BASE ADJUST Control

Used with Options 03, 04, or 05 only. Screwdriver adjustment allows tuning of the internal 10 MHz Oven Oscillator used with these options. Refer to Section O for complete description.

TIME BASE INT/EXT Switch

Allows use of internal Time Base Oscillator (TCXO or optional oven unit), or external 10 MHz reference.

TIME BASE 10 MHz Connector

Type BNC female. Allows monitoring of internal 10 MHz Time Base, or connection to external 10 MHz reference (3 V p-p maximum reference input level).

BCD OUTPUT Connector

Used with Option 09 - BCD Output. Refer to Section O - Options, for complete description.

REMOTE PROGRAMMING Connector

Used with Option 06 - Programmable Offsets, and Option 07 - Remote Programming. Refer to Section O - Options for complete descriptions.

AC POWER Connector

Accepts AC power cord supplied with counter.

FUSE Holder

Fuse provides overload protection for the counter. Use only a 1.5 A, Slow-Blow, 3AB/MDX type fuse for nominal 115 Vac operation, or 0.75 A, Slow-Blow, 3AB/MDL type fuse for nominal 230 Vac operation.

115/230 Switch

Sets operating voltage of counter to match power line. CAUTION: Be sure 115/230 switch setting and fuse rating match power line voltage.

TABLE 3-2. REAR PANEL CONTROLS AND CONNECTORS

IMPORTANT: Erroneous readings may result for signals within 275 MHz above and below the YIG Preset frequency. Set YIG Preset at least 275 MHz *below* lowest desired frequency to be counted.

3-12. To utilize both YIG Preset and lockbox functions of the counter simultaneously, proceed as follows:

a. Program YIG Preset frequency. Press **PRESET** button.

b. Wait for **SEARCH** indicator to go out.

c. Source may now be locked as described in paragraph 3-8c.

SECTION 4

GENERAL THEORY OF OPERATION

4-1. GENERAL

4-2. The EIP 371 Source Locking Microwave Counter automatically measures and displays the frequency of any CW signal from 20 Hz to 18.0 GHz. This frequency coverage is obtained in three bands: 20 Hz - 300 MHz (Band I), 100 MHz - 850 MHz (Band II), and 825 - 18 GHz (Band III). In addition, the 371 has the capability of locking a frequency modulatable source to any 100 kHz increment between 10 MHz and 18 GHz.

4-3. Measurements in Band I are made directly with a 300 MHz counter. This band is further divided into two channels: Channel A covers the 20 Hz - 135 MHz range with an input impedance of 1 megohm shunted by 20 pf. Channel B covers the 10 MHz - 300 MHz range with a 50 ohm input impedance.

4-4. Band II contains a prescaler which divides the input frequency by four. It operates over the frequency range of 100 MHz - 850 MHz with 50 ohm input impedance.

4-5. Band III covers the microwave frequencies from 825 MHz - 18 GHz with a 50 ohm input impedance. In this band, an Autohet Converter translates the input frequency downward into the frequency range of the 300 MHz Direct Counter. This is accomplished by mixing the input signal with a single known harmonic of the counter time base oscillator, to produce a difference frequency which can be counted directly. The frequency of the known harmonic is added to the counted signal to obtain the input frequency.

4-6. Figure 4-1 shows a block diagram of the complete 371 Counter. Figure 4-2 shows a block diagram of the Autohet Converter. Detailed theory and circuit descriptions of the Counter and Converter subassemblies are given in Section 9.

4-7. The operation of the 371 Counter is best described by separating the instrument into three distinct functions: the Direct Counter, the Autohet Converter, and the Lockbox circuitry. The Direct Counter and the Autohet Converter are interconnected in two significant areas: (1) presetting the counter to the appropriate harmonic number, and (2) counting the heterodyned difference frequency from the Converter by the Direct Counter.

4-8. 300 MHz DIRECT COUNTER

4-9. The measurement of frequency by the direct counter is accomplished by accumulating the number of input events (e.g: cycles of a sine wave), which occur within a precisely determined time interval. This time interval is based on the frequency of the Time Base Oscillator.

4-10. The 20 Hz - 300 MHz portion of the counter is separated physically into a number of subassemblies, designated A101 through A111 (refer to Figure 4-1, Block Diagram). The subassemblies are tied together via the Counter Interconnect Board A113. The counter is divided functionally in approximately the same manner as it is divided into subassemblies. Count Chain Boards A101, A102, and A103, operate functionally as a single unit, as do Control Boards A104 and A105. The principal interconnections between the units are shown in Figure 4-1.

4-11. Band I (20 Hz - 300 MHz) input has two operating modes. Band IA covers the 20 Hz - 135 MHz range, with 1 megohm/20 pf input impedance and 25 mV rms sensitivity. Band IB (10 MHz - 300 MHz) has a 50 ohm input impedance and -20 dBm sensitivity. Both Band IA and IB input signals are routed through Preamplifier A111, which contains an impedance converter section and a signal amplifier to drive the High Frequency board (A106).

4-12. The Band II (100 MHz - 850 MHz) input drives the Prescaler (A109), which divides the incoming frequency by four and routes it to the High Frequency Board.

4-13. The signal input to Band III (825 MHz - 18.0 GHz) is translated by the Autohet Converter into the range of 25 MHz - 275 MHz, and routed to the High Frequency board (A106).

4-14. The outputs of these three input signal processors thus fall between 20 Hz and 300 MHz; the frequency range of the direct counter. The individual assemblies which comprise the direct counter are described in general terms below, and in detail in Section 9.

4-15. The High Frequency Board (A106) receives the input signal from one of the processors, squares the signal, and forms it into a train of constant duration pulses. This pulse train frequency is then divided by ten, and sent to the Count Chain.

4-16. The Control 1 and Control 2 Boards (A104 and A105), contain circuitry to guide the counter through the steps necessary to acquire and display the input frequency. The circuits control the opening and closing of the signal gate in the High Frequency Board, and accept programming commands from the Converter, front panel controls (TEST, RESET, SAMPLE RATE), and the Remote Programming options.

4-17. The Count Chain Boards (A101, A102, and A103), accumulate the frequency from the High Frequency Board, store the accumulated information, and multiplex the stored information into a form usable by the Display Board (A110), which provides a visual display of the input frequency to the counter.

4-18. Reference Oscillator Buffer A108, produces a time base reference signal from either an internal 10 MHz oscillator, or an external 10 MHz source. All input frequencies to the counter are measured with respect to this signal.

4-19. The Power Supply (A107) provides regulated +12,

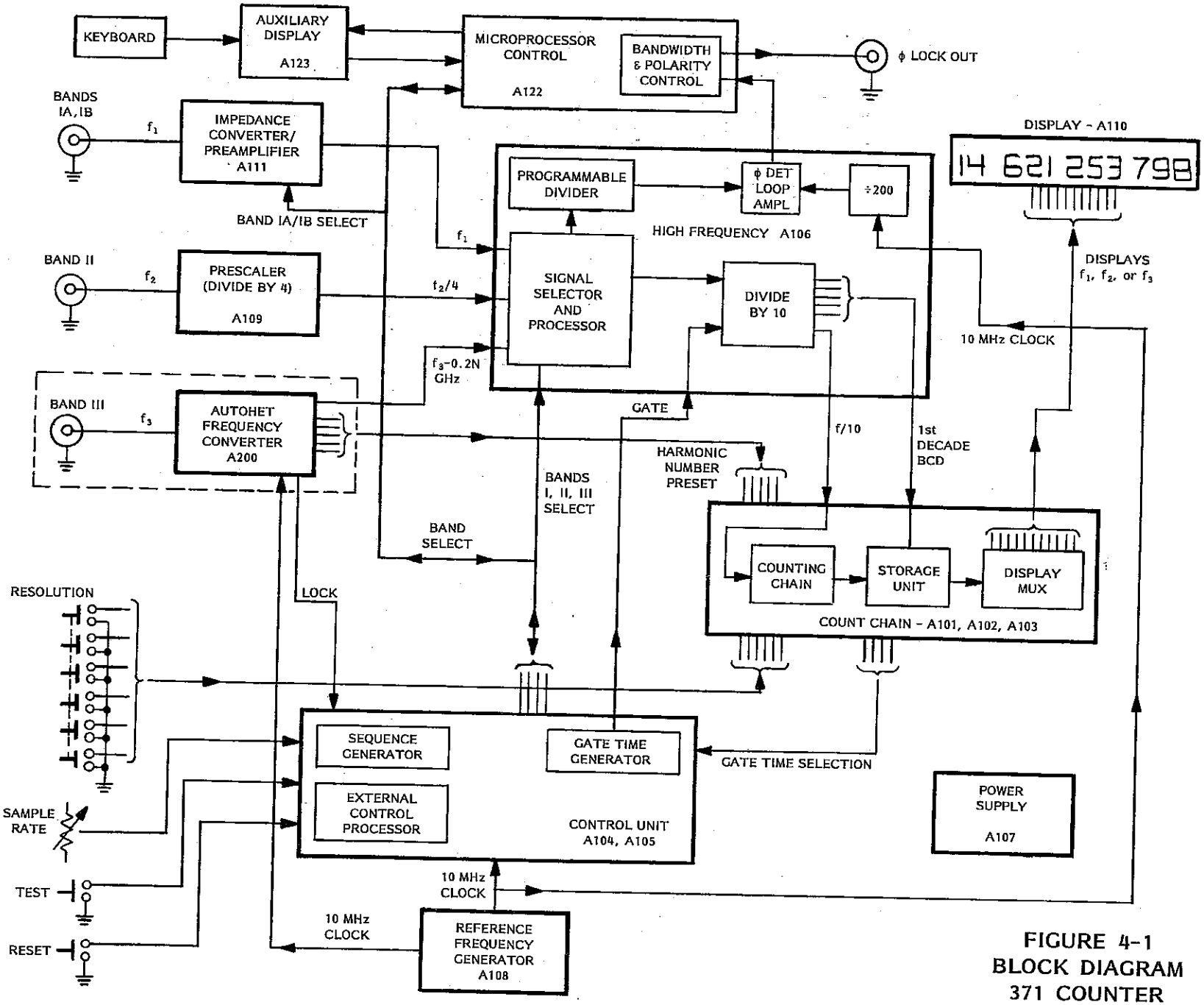


FIGURE 4-1
BLOCK DIAGRAM
371 COUNTER

-12, +5, -5.2 Vdc, and unregulated +18 Vdc. NOTE: This supply does not furnish the power for the oven stabilized Time Base Oscillators (Options 03, 04, or 05).

4-20. AUTOHET CONVERTER

4-21. The Autohet Converter is a self-contained assembly which performs the function of translating the microwave frequencies appearing at the Band III input, down into the range of the direct counter. This translation is accomplished by mixing the incoming signal with a known reference signal and then amplifying the difference frequency. The incoming frequency is then determined by counting the difference frequency and adding it to the known reference frequency. Refer to Figure 4-2, Converter Block Diagram.

4-22. The reference frequency is an integral multiple of 200 MHz which is derived from the 10 MHz Time Base Oscillator, thus maintaining the basic counter accuracy in the microwave band.

4-23. The Band III input signal passes through the PIN Diode Attenuator (A206) and is combined in the Mixer (A205) with the reference frequency from the YIG/Comb Generator.

4-24. The YIG/Comb Generator (A207) is an integrated assembly containing a Comb Generator and a YIG filter. The Comb Generator contains a step recovery diode to convert the 200 MHz sine wave input from the Source/-Amplifier (A201) into a train of narrow pulses containing all the harmonics of 200 MHz up to 18 GHz. This pulse train is then passed through a pair of YIG resonators which select the desired harmonic. The resonant frequency of the two stage filter is proportional to a magnetic field generated by passing current through a pair of coils within the structure. (A more comprehensive description of the operation of a YIG-tuned device is given later in this section.)

4-25. The Source Amplifier (A201) contains an LC oscillator operating at 200 MHz, which is phase-locked to the 10 MHz Time Base Oscillator (A116 or A112). This 200 MHz signal is amplified to produce up to one watt of output power to drive the Comb Generator section of A207.

4-26. The Mixer (A205) is an integrated microwave stripline assembly, containing a 3 dB hybrid coupler, a termination, a mixer diode, a matching network, a broadband DC return, and a bypass capacitor to separate the RF and IF signals. The Mixer produces two output signals: an IF signal with frequency equal to the difference of the reference and incoming signals, and a DC current resulting from rectification of the total power applied to the mixer diode.

4-27. Both the IF and DC signals from A205 enter Video Amplifier A204, where the IF signal is amplified, and the DC level used for control of PIN Diode Attenuator A206.

4-28. The circuitry required to control the Autohet Converter is located on two Converter Control Boards (A202 and A203). Their function is to set the YIG Filter within the YIG/Comb Generator (A207) to the correct harmonics of 200 MHz, and to provide both the IF frequency and the harmonic information to the Direct Counter.

4-29. To accomplish this, the YIG Filter passband is continuously tuned over the operating range until an appropriate signal is received from the Video Amplifier. The sweep is then stopped so the YIG Filter passband is centered on the desired harmonic. Converter Control 1 (A203) performs all the signal processing and provides digital commands to Converter Control 2 (A202) which contains the Digital to Analog Converters and the current driver necessary to tune the YIG Filter. A detailed operational sequence is described in Section 9 in the Converter Control 1 description (Figure 9-17).

4-30. LOCKBOX OPERATION

4-31. The source locking (lockbox) portion of the counter consists of three assemblies: the High Frequency board (A106), the Microprocessor board (A122), and the Auxiliary Display board (A123).

4-32. The High Frequency board selects the appropriate input signal, processes it, and divides it into two signals: one drives the gating and first stage of the frequency counting portion of the counter, while the other signal drives the phase locking portion.

4-33. The phase locking portion of the High Frequency board divides the selected signal down to 50 kHz in a programmable frequency divider. The 50 kHz signal is compared with a 50 kHz reference signal — derived from the 10 MHz time base clock — in a phase comparator, producing an error signal proportional to the phase (frequency) difference between the two signals. This error signal is sent to the Microprocessor board (A122) for amplification and processing, and then sent out to the signal source to correct for phase (frequency) errors.

4-34. The Microprocessor (A122) performs several tasks, including control of the Auxiliary Display board (A123). The Microprocessor interprets and processes the keyboard entries, and displays the appropriate data on the Auxiliary Display. It also controls the LOCK and PRESET indicators, and the BAND SELECT function (and indicators), in accordance with the appropriate keyboard entry commands.

4-35. In performing the YIG Preset function, the Microprocessor justifies the programmed frequency data to a multiple of 0.2 GHz, and then sends the data to the Converter Control 2 board (A202).

4-36. In performing the Lock command, the Microprocessor collects frequency information from the Converter and keyboard entries, and determines if a lock is possible. If so, it computes the IF frequency which should be present in the High Frequency board, and programs the frequency divider to generate the 50 kHz signal for the phase comparator. In Band II operation, it also justifies the frequency to be the proper multiple of 400 kHz (due to prescaler requirements).

4-37. Part of the lock operation is the selecting of loop gain (loop bandwidth) and polarity. The Microprocessor board perform this task by systematically programming gain and polarity information, and sampling the loop lock and bandwidth data. When the appropriate gain is reached, and both lock and bandwidth are correct, the processor returns to the keyboard/display scan. If a lock is not achieved, the processor returns to the keyboard/-display scan with the phase lock control voltage returned to zero volts.

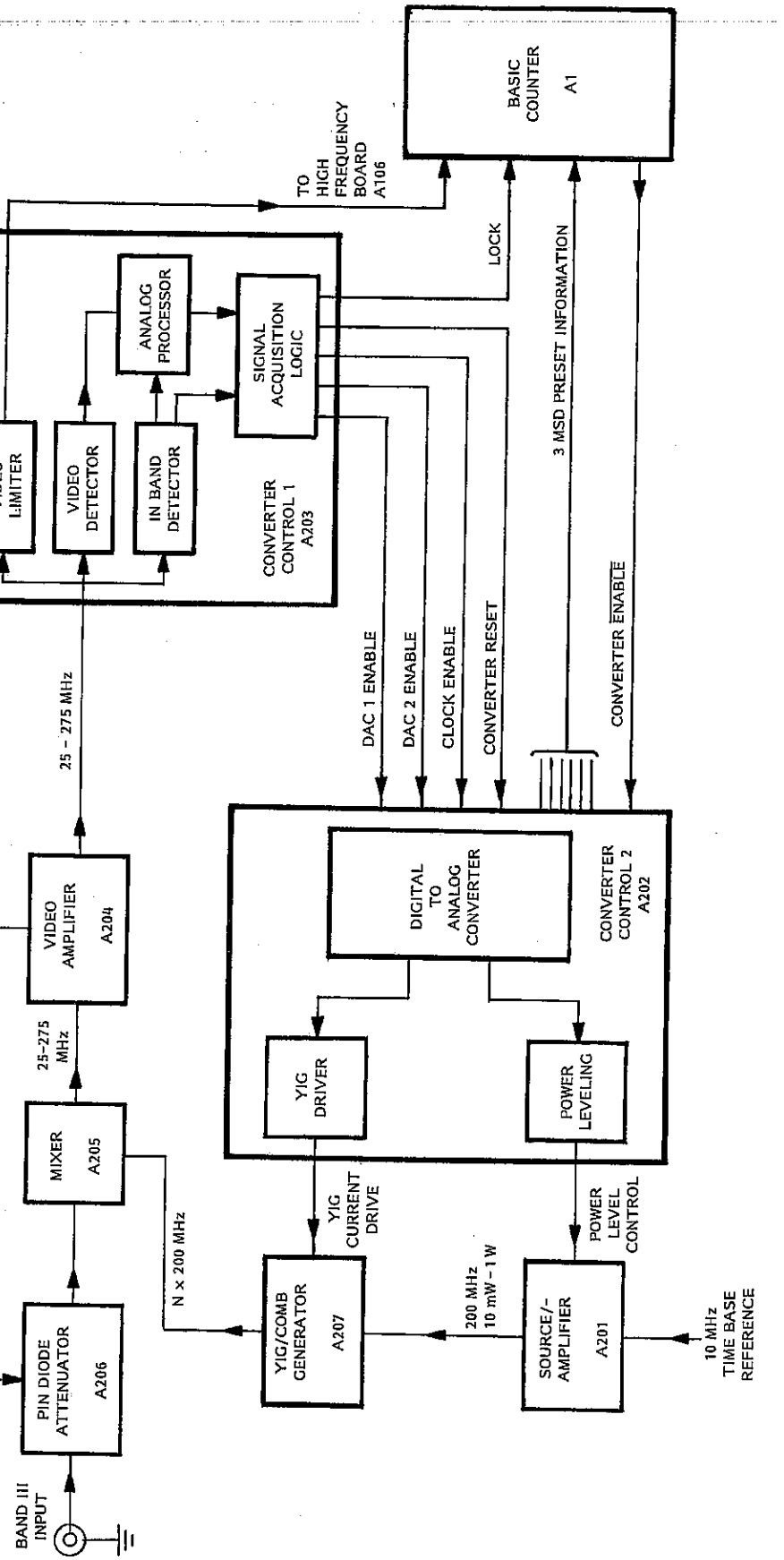


FIGURE 4-2
BLOCK DIAGRAM
AUTOHET CONVERTER

AN INTRODUCTION TO YIG FILTERS

Highly polished spheres of single crystal YIG (yttrium-iron-garnet), have a property called ferrimagnetic resonance. Basically, the ferrimagnetic resonance phenomenon can be explained in terms of spinning electrons creating a net magnetic moment in each molecule of a YIG crystal (see Figure A). Viewing the material macroscopically, there is no net effect because the magnetic dipoles associated with each molecule are randomly oriented (see Figure B). The application of an external magnetic biasing field, H_{DC}, causes the magnetic dipoles to be aligned in the direction of the biasing field (see Figure C).

An RF field can be used to create an orthogonal magnetic force. If the frequency of the RF field coincides with the natural precession frequency, there is a strong interaction called ferrimagnetic resonance (Figure D).

Figure E shows the basic elements of a YIG bandpass filter. The filter consists of a YIG sphere at the center of two loops. The two loops are perpendicular to each other and to the dc biasing field, H_{DC}. One loop carries the RF input and the other the RF output. When the RF signal frequency is the same as the natural precession frequency of the YIG, there is strong coupling between the input and output loops. Thus RF can only pass through the YIG filter at resonance. The resonant frequency is a linear function of the magnetic biasing field, H_{DC}. Generally, H_{DC} is provided by locating the YIG spheres between the poles of an electromagnet, and tuned by varying the current to the magnetic coils.

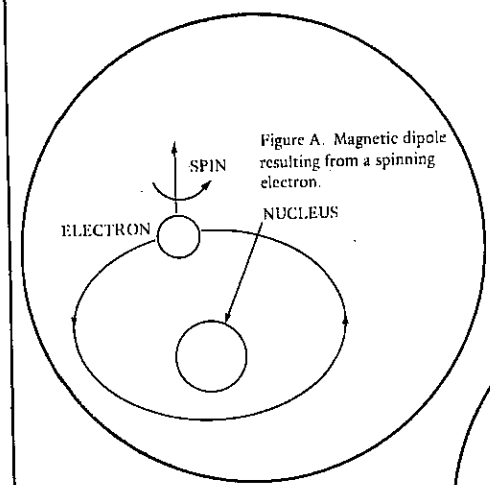


Figure A. Magnetic dipole resulting from a spinning electron.

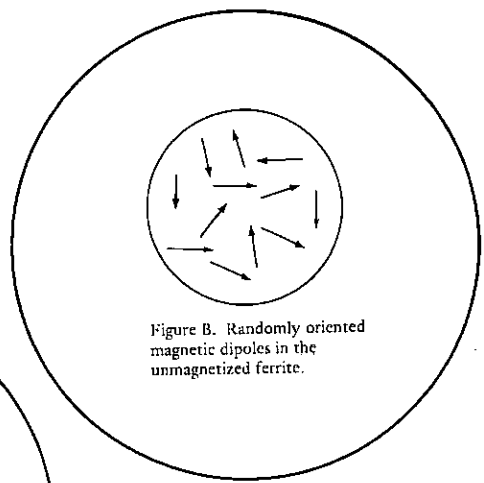


Figure B. Randomly oriented magnetic dipoles in the unmagnetized ferrite.

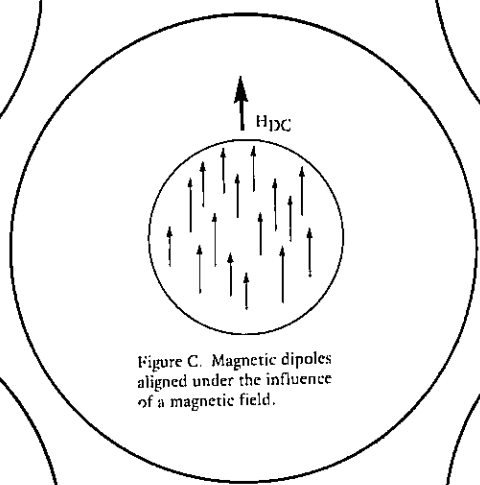


Figure C. Magnetic dipoles aligned under the influence of a magnetic field.

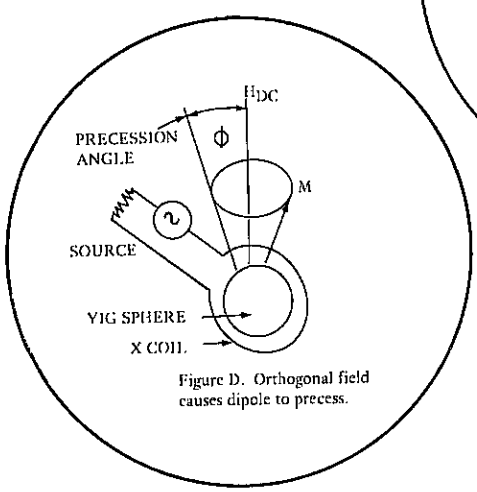


Figure D. Orthogonal field causes dipole to precess.

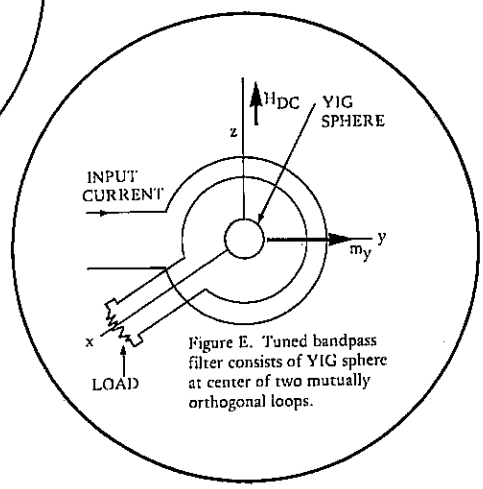


Figure E. Tuned bandpass filter consists of YIG sphere at center of two mutually orthogonal loops.

SECTION 5

MAINTENANCE & SERVICE

5-1. GENERAL

5-2. This section provides instructions, procedures, and information necessary to maintain, troubleshoot, and repair the EIP Autohet Microwave Counter.

5-3. FUSE REPLACEMENT

5-4. The counter uses one fuse, located on the rear panel. For proper operation, use only the fuse specified below; do not increase fuse rating or change fuse type. Set 115/230 slide switch on rear panel to match nominal power line voltage.

For 115 VAC operation: use a 1.5A, Slow-Blow, 3AB/MDX type fuse.

For 230 VAC operation: use a 0.75A, Slow-Blow, 3AB/MDL type fuse.

5-5. AIR CIRCULATION

5-6. During operation of the counter, the internal fan draws in cooling air through the vents in the enclosure. If these vents are blocked, the temperature inside the enclosure may rise to the point where counter stability is reduced, and component life shortened.

5-7. COUNTER SERVICING

5-8. Recommended Service Procedures:

a. To remove plug-in PC Boards: Ease board out of socket by lifting up on board handles. Remove carefully to avoid placing strain on any connecting cables.

b. To unplug flat ribbon cables: Turn off power to counter. Use an IC Extractor Tool (EIP Part 5000094 or equivalent) to unplug connector.

c. To remove PCB socket locating key: Key must be turned 90° before removal from or re-installation into socket, to avoid contact damage. Use long-nose pliers for removal or insertion.

d. A Troubleshooting Kit (EIP Part 2000005) is available to facilitate adjustments and repairs of the counter. Contents include PCB Extender Cards, IC Removal Tool, Summing Amplifier, adapter cables and connectors.

e. Internal cable and harness routing is shown both on a label attached to the top cover of the counter, and in Figure 9-2.

f. Circuit descriptions of PC Board and modular assemblies are shown on the same pages as the related schematic diagram and component locator in Section 9.

g. Troubleshooting Trees shown later in this section are intended only as a guide, and do not describe every possible failure situation. To speed troubleshooting of a board: replace the board with a known good one.

h. A listing of recommended test equipment for servicing, calibration, and performance testing, is given in Table 5-1. Other equipment may be used provided performance equals or exceeds that listed.

i. A Schematic Diagram of a Summing Amplifier used in certain counter tests, is shown in Figure 5-1. This unit may be constructed by the user, or may be purchased directly from EIP (Part Number 2010050).

5-9. Servicing Precautions

a. The Video Amplifier (A204) and the Source/Amplifier (A201) should be replaced rather than being serviced in the field, due to the specialized test equipment and procedures required for recalibration.

b. If Converter Control 2 (A202) is repaired either at EIP or in the field, recalibration in its associated counter will be required for proper counter operation.

> CAUTION
>
> DO NOT ATTEMPT REPAIR OR DISASSEMBLY OF THE FOLLOWING COMPONENTS: YIG/COMB GENERATOR (A207), MIXER (A205), INPUT ATTENUATOR (A206), OR TIME BASE OSCILLATOR (TCXO OR OVEN OPTION).

5-10. FACTORY SERVICE

5-11. If the counter is to be returned to EIP for service or repair, BE SURE TO INCLUDE THE FOLLOWING INFORMATION WITH THE SHIPMENT: *

a. Name and address of owner.

b. Model and complete serial number of counter.

c. A COMPLETE description of trouble (e.g: under

EQUIPMENT DESCRIPTION	MFR.	MODEL	Section 5 - Service	Section 6 - Calibration	Section 7 - Performance
Signal Source: (1) 20 Hz - 10 MHz	HP	651B	x		x
(2) 10 MHz - 1 GHz	Wavetek	2001B	x	x	x
(3) 1 GHz - 12.4/18 GHz	S-D	521-series	x	x	x
Oscilloscope (Main Frame)	HP	180C	x	x	
Dual Channel Ampl. (Plug-In)	HP	1801A	x	x	
Delayed Time Base (Plug-In)	HP	1821A	x	x	
Digital Voltmeter ($4\frac{1}{2}$ digit)	Dana	4800	x	x	
Power Meter	HP	432B	x	x	x
Thermistor Mount (10 MHz-18 GHz)	HP	8478	x	x	x
Frequency Standard	HP	105A		x	
VLF Comparator	HP	117A		x	
Summing Amplifier *	EIP	2010050*	x	x	
Variable 115 Vac Source	Staco	3PN501			x
Extender Card	EIP	2020021	x	x	
Adapter Cable (SMC to BNC)	EIP	2040015	x	x	
Misc. attenuators, adapters and cables			x	x	x

* See Figure 5-1.

TABLE 5-1. RECOMMENDED TEST EQUIPMENT

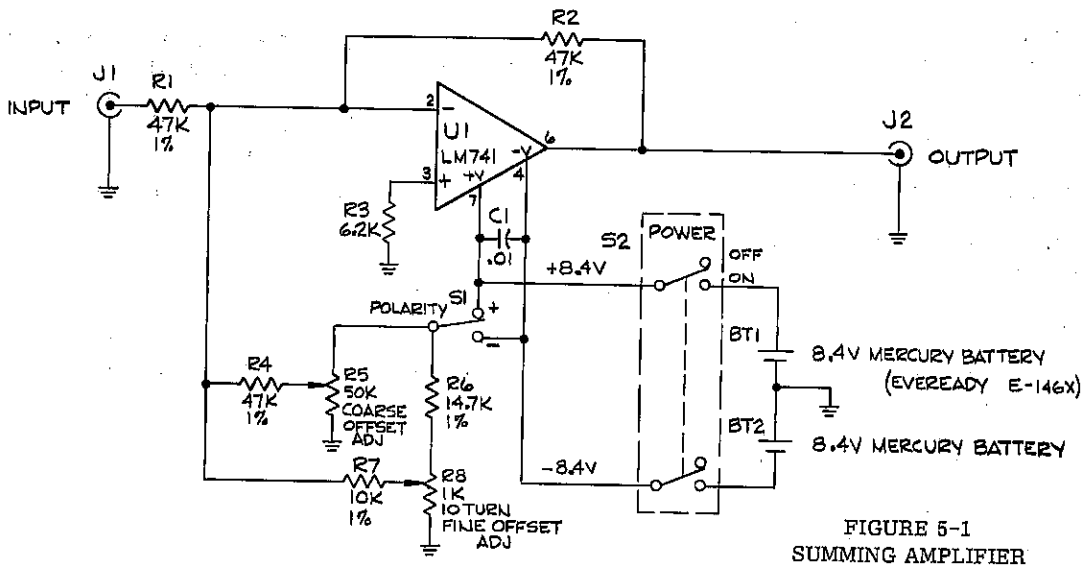


FIGURE 5-1
SUMMING AMPLIFIER

what conditions did trouble occur? What was the signal level? What associated equipment was attached or connected to the counter? Did that equipment fail too?)*

d. Name and telephone number of someone familiar with the problem, who may be contacted by EIP for any further information if necessary.

e. Shipping address to which counter is to be returned; include any special shipping instructions.

f. Pack the counter as follows:

(1) Wrap the counter in plastic or heavy kraft paper, and repack in the original shipping container (if still available) using the original packing material.

(2) If the original container and packing material are no longer available, use a heavy (275 lb. test) double-walled carton, with approximately 4" of suitable packing material between the inner and outer walls, with additional packing material as required between the counter and the inner carton. Seal with strong filamentary tape or strapping.

(3) Mark the shipping container to indicate that it contains fragile electronic instruments. Ship to EIP at address shown on title page of this manual.

* A COUNTER REPAIR AND RETURN FORM IS BOUND INTO THE BACK OF THIS MANUAL. IF THE FORM IS MISSING, PLEASE SUPPLY THE INFORMATION REQUESTED IN THE ABOVE PARAGRAPH.

5-12. TROUBLESHOOTING

5-13. MALFUNCTION AT TURN ON

5-14. If the counter fails to turn on (no display, no fan, etc.), make the following checks:

a. 115/230 switch at proper setting.

b. Power cord plugged into counter and into AC power source.

c. Correct AC power available at source.

d. Counter fuse good.

e. POWER switch at "On" position (button depressed and green indicator showing).

f. PC Boards and connectors are properly engaged.

g. Counter power supply voltages correct (measured on Counter Interconnect PC Board A113).

5-15. FAILURE TO INDICATE ALL ZEROS

5-16. If counter turns on, but fails to indicate all zeros with no applied signal, CHECK THAT:

a. No RESOLUTION switches are depressed.

b. INT/EXT switch is set to INT.

c. PC Boards and connectors are properly engaged.

d. Counter Power Supply (A107) voltages correct.

e. Perform Visual Display Test by pressing TEST and RESET switches simultaneously; display should show "8" in all decade positions.

f. If counter fails the Visual Display Test, refer to Troubleshooting Tree - Figure 5-2. If counter displays all eights but a digit is missing, refer to Figure 5-3. If the display does not show all zeros when it should, refer to Figure 5-4.

5-17. MALFUNCTION IN SELF TEST

5-18. If counter turns on, but fails to indicate a reading of 10 000 000 (10 MHz) in the TEST mode, CHECK THAT:

a. Counter indicates all zeros with no applied signal.

b. PC Boards and connectors are properly engaged.

c. Counter Power Supply (A107) voltages correct.

d. Counter passes Visual Display Test (para. 5-16).

e. Refer to Figure 5-5.

5-19. MALFUNCTION IN BAND IB (10 MHz to 300 MHz)

5-20. If counter fails to read frequency correctly, CHECK THAT:

a. Counter is set to Band IB (10 MHz - 300 MHz position).

b. A signal is applied to the Band I input connector. The signal level and frequency should be as specified for Band IB.

c. If signal input is correct, counter should indicate all zeros when signal is removed. If not, refer to paragraph 5-16.

d. Counter passes Visual Display Test (para.5-16).

e. Counter operates correctly in TEST mode. If not, refer to paragraph 5-18.

f. Refer to Figure 5-6.

5-21. MALFUNCTION IN BAND IA
(20 Hz to 135 MHz)

5-22. If counter fails to read frequency correctly, CHECK THAT:

a. Counter is set to Band IA (20 Hz - 135 MHz position).

b. A signal is applied to the Band I input connector. The signal level and frequency should be as specified for Band IA.

c. If signal input is correct, counter should indicate all zeros when signal is removed. If not, refer to paragraph 5-16.

d. Counter passes Visual Display Test (para. 5-16).

e. Counter operates correctly in TEST mode. If not, refer to paragraph 5-18.

f. Counter operates properly in Band IB.

g. Refer to Figure 5-7.

5-23. MALFUNCTION IN BAND II
(100 MHz to 850 MHz)

5-24. If counter fails to read frequency correctly, CHECK THAT:

a. Counter is set to Band II (100 MHz - 850 MHz position).

b. A signal is applied to the Band II input connector. The signal level and frequency should be as specified for Band II.

c. If signal input is correct, counter should indicate all zeros when signal is removed. If not, refer to paragraph 5-16.

d. Counter passes Visual Display Test (para. 5-16).

e. Counter operates correctly in TEST mode. If not, refer to paragraph 5-18.

f. Prescaler PC Board (A109) connector and co-ax cables properly engaged.

g. Counter operates properly in Band IB.

h. Refer to Figure 5-8.

5-25. MALFUNCTION IN BAND III
(825 MHz to 18 GHz)

5-26. If counter fails to read frequency correctly, CHECK THAT:

a. Counter is set to Band III (825 MHz - 18 GHz position.

b. A signal is applied to the Band III input connector. The signal level and frequency should be as specified for Band III.

c. If signal input is correct, counter should indicate all zeros when signal is removed. If not, refer to paragraph 5-16.

d. Counter passes Visual Display Test (para. 5-16).

e. Counter operates correctly in TEST mode. If not, refer to paragraph 5-18.

f. Counter operates properly in Bands I and II.

g. Converter Control (A202 and A203) PC Board connectors and co-ax cables are properly engaged.

h. Refer to Figure 5-9.

5-27. LOCKBOX MALFUNCTION

5-28. If counter fails to lock, CHECK THAT:

a. Programmed frequency matches related counter operating band.

b. Programmed frequency is within specific capture range.

c. Phase Lock Out signal is connected to the FM or phase lock input of the source being locked.

d. Source being locked has an FM or phase lock input which meets the requirements of the 371.

e. Refer to Figure 5-10.

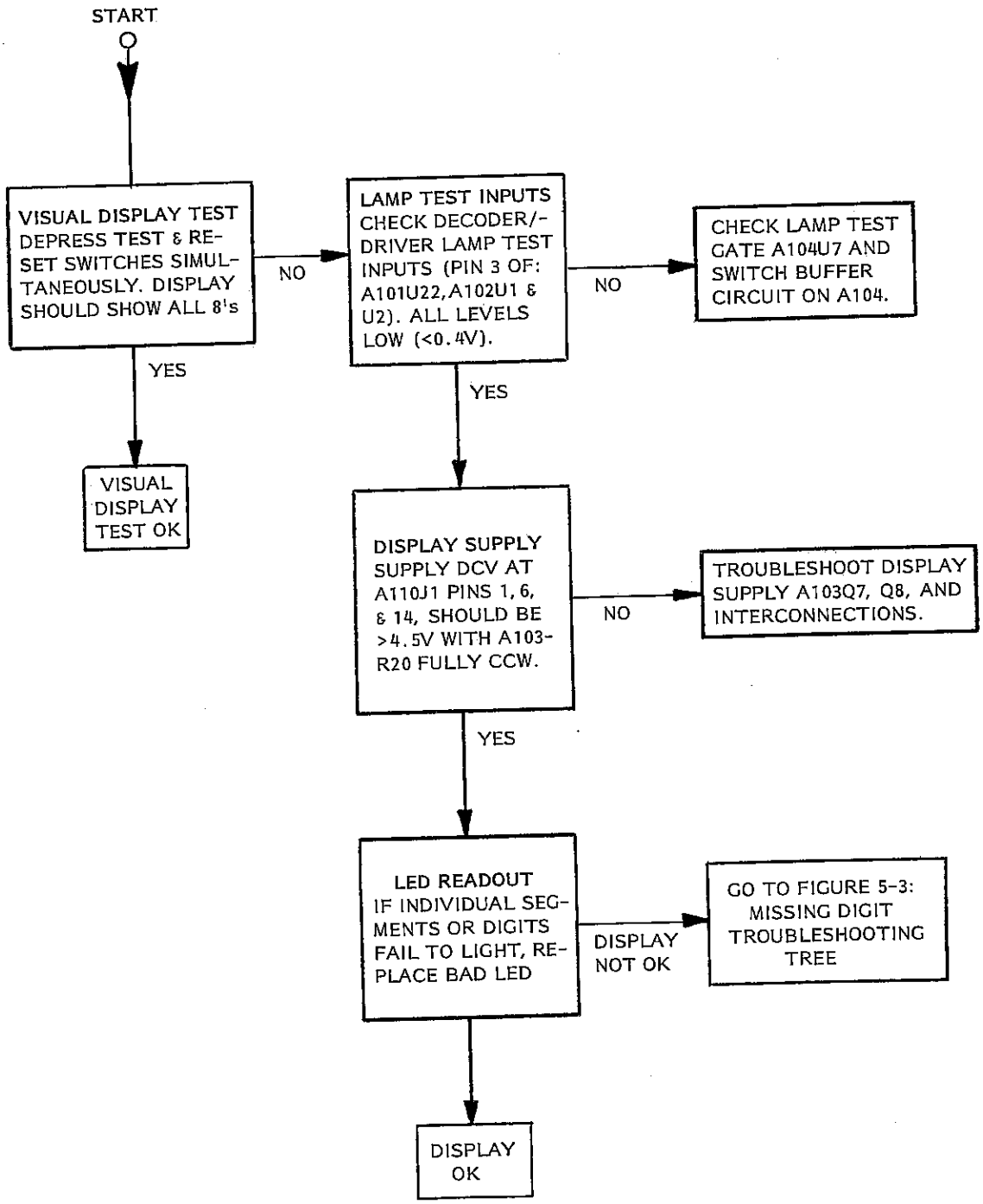


FIGURE 5-2
VISUAL DISPLAY TEST
TROUBLESHOOTING TREE

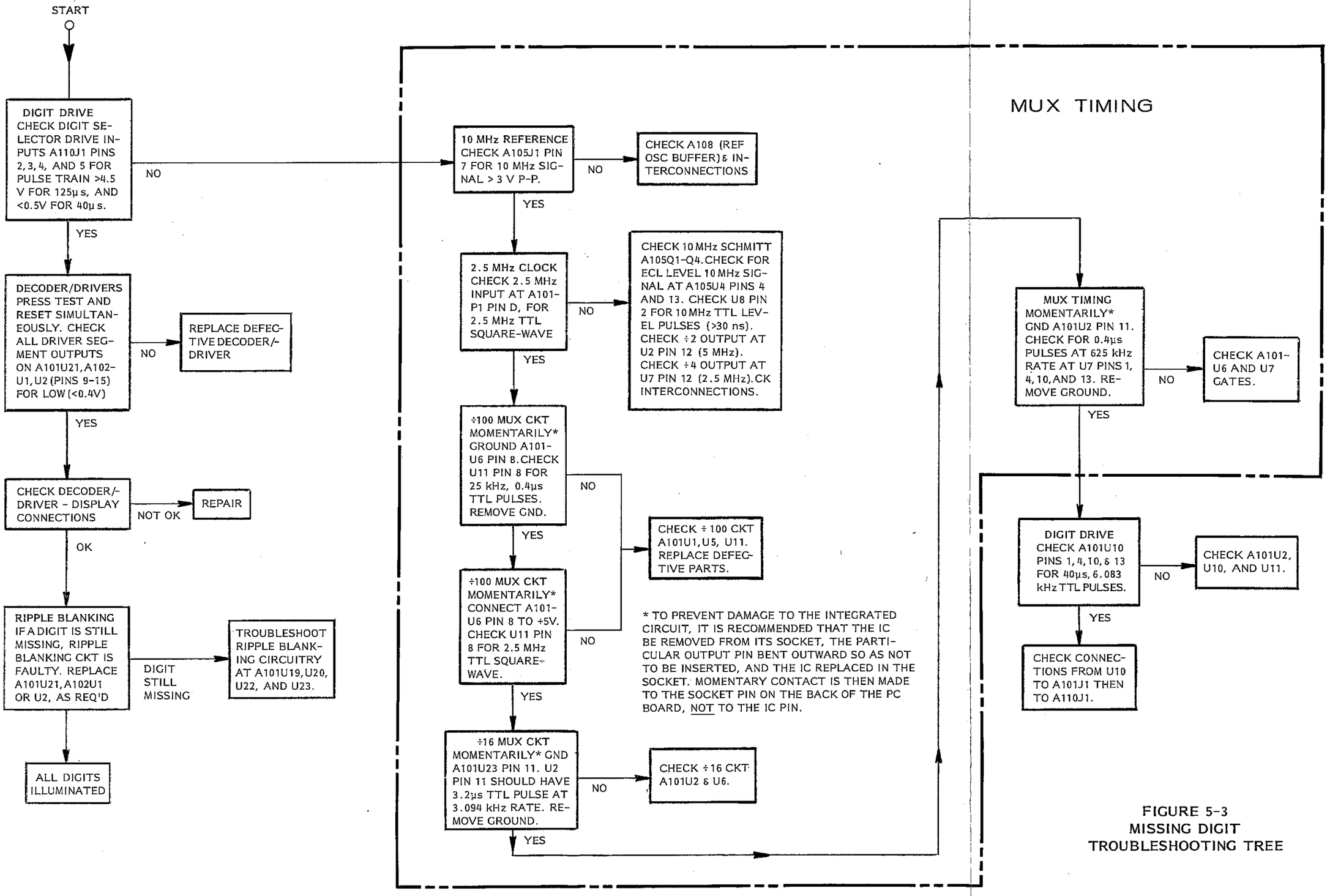


FIGURE 5-3
MISSING DIGIT
TROUBLESHOOTING TREE

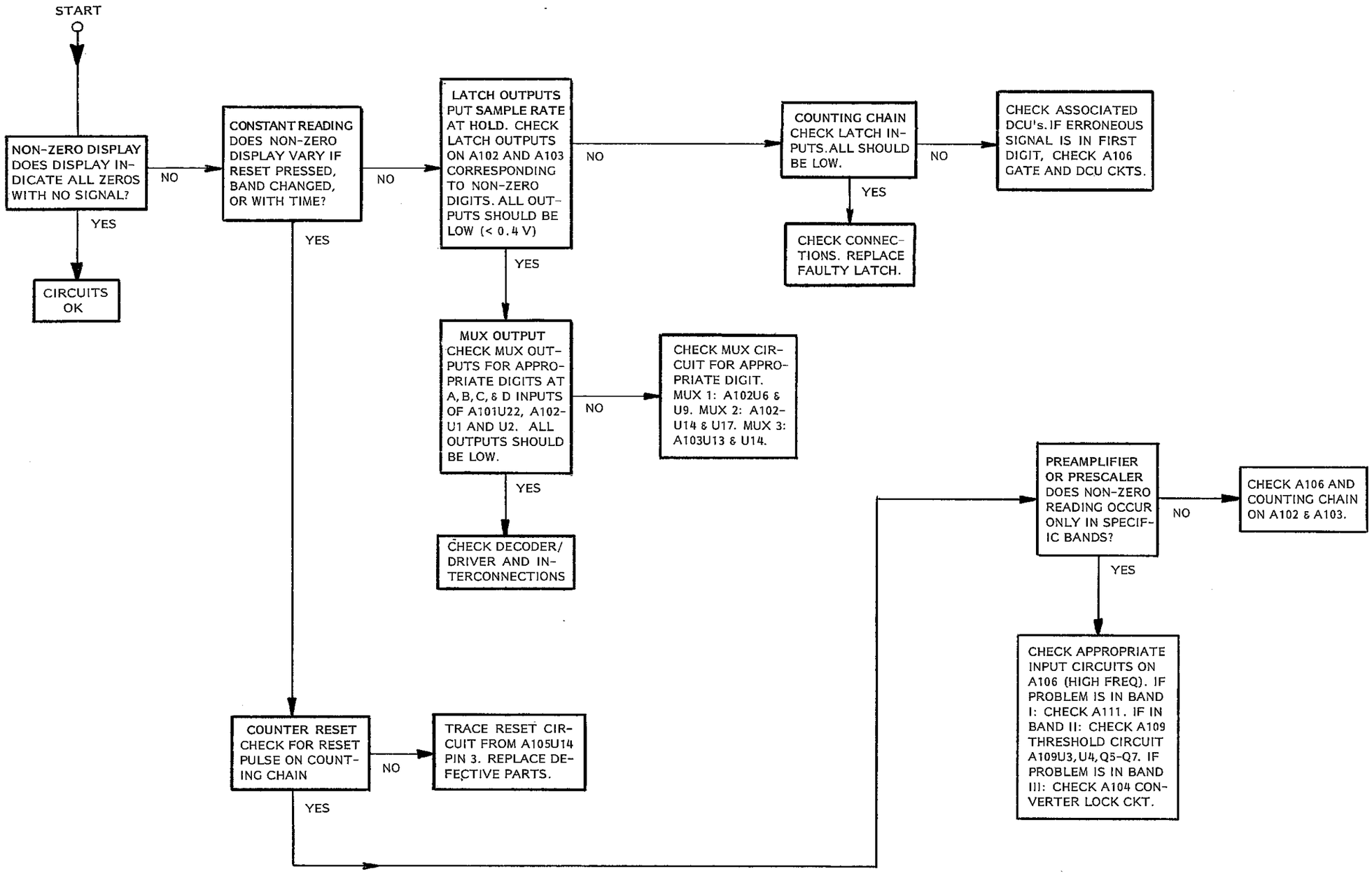


FIGURE 5-4
NON-ZERO DISPLAY
TROUBLESHOOTING TREE

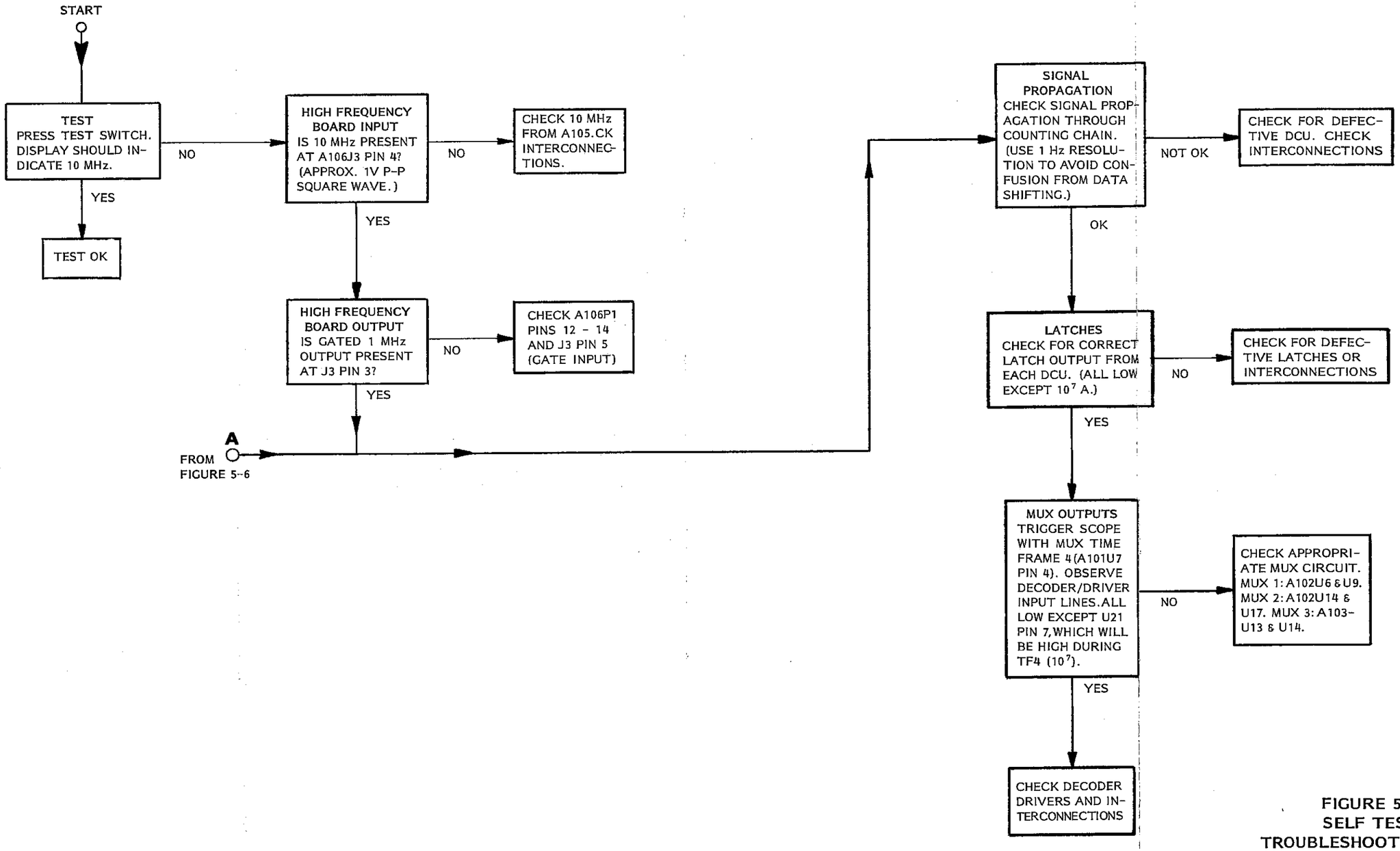
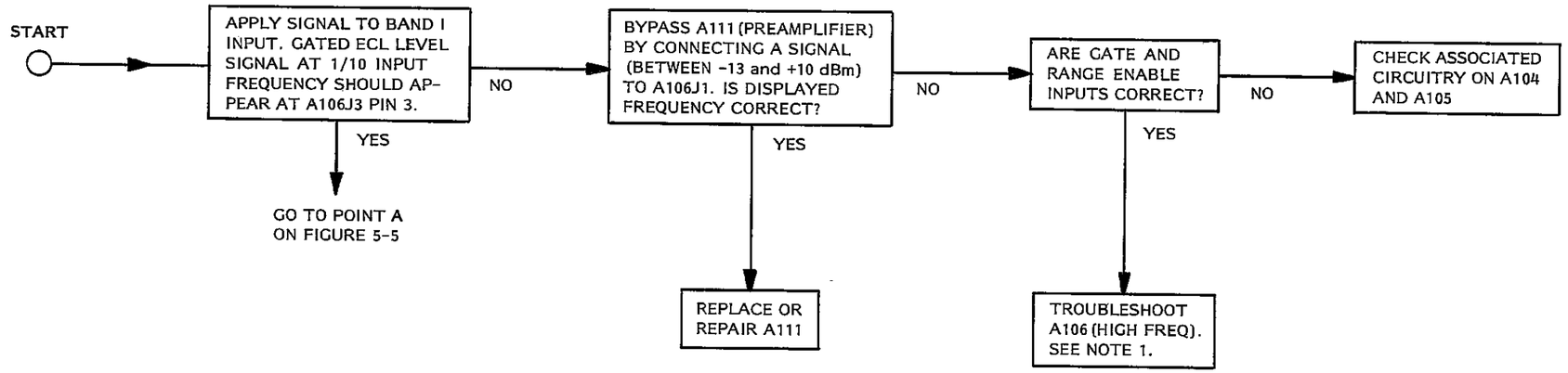


FIGURE 5-5
SELF TEST
TROUBLESHOOTING TREE



NOTE 1: TROUBLESHOOTING OF A106 REQUIRES USE OF A SAMPLING OSCILLOSCOPE WITH A 1 GHz OR GREATER BANDWIDTH. CARE MUST BE EXERCISED TO LOAD CIRCUIT JUNCTION LIGHTLY. MAXIMUM PROBE CAPACITANCE: 1 PF. MINIMUM RESISTANCE: 500 OHMS.

FIGURE 5-6
BAND IB
TROUBLESHOOTING TREE

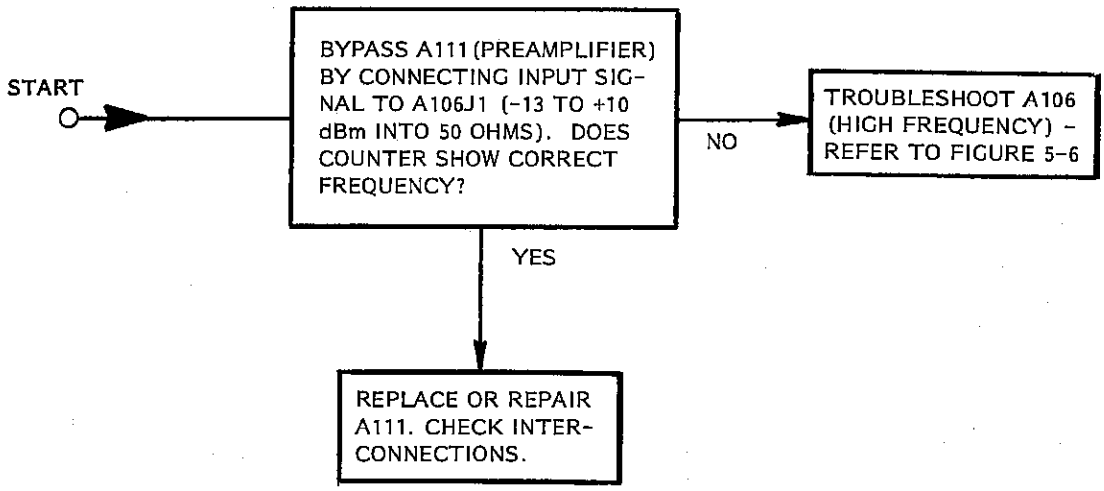
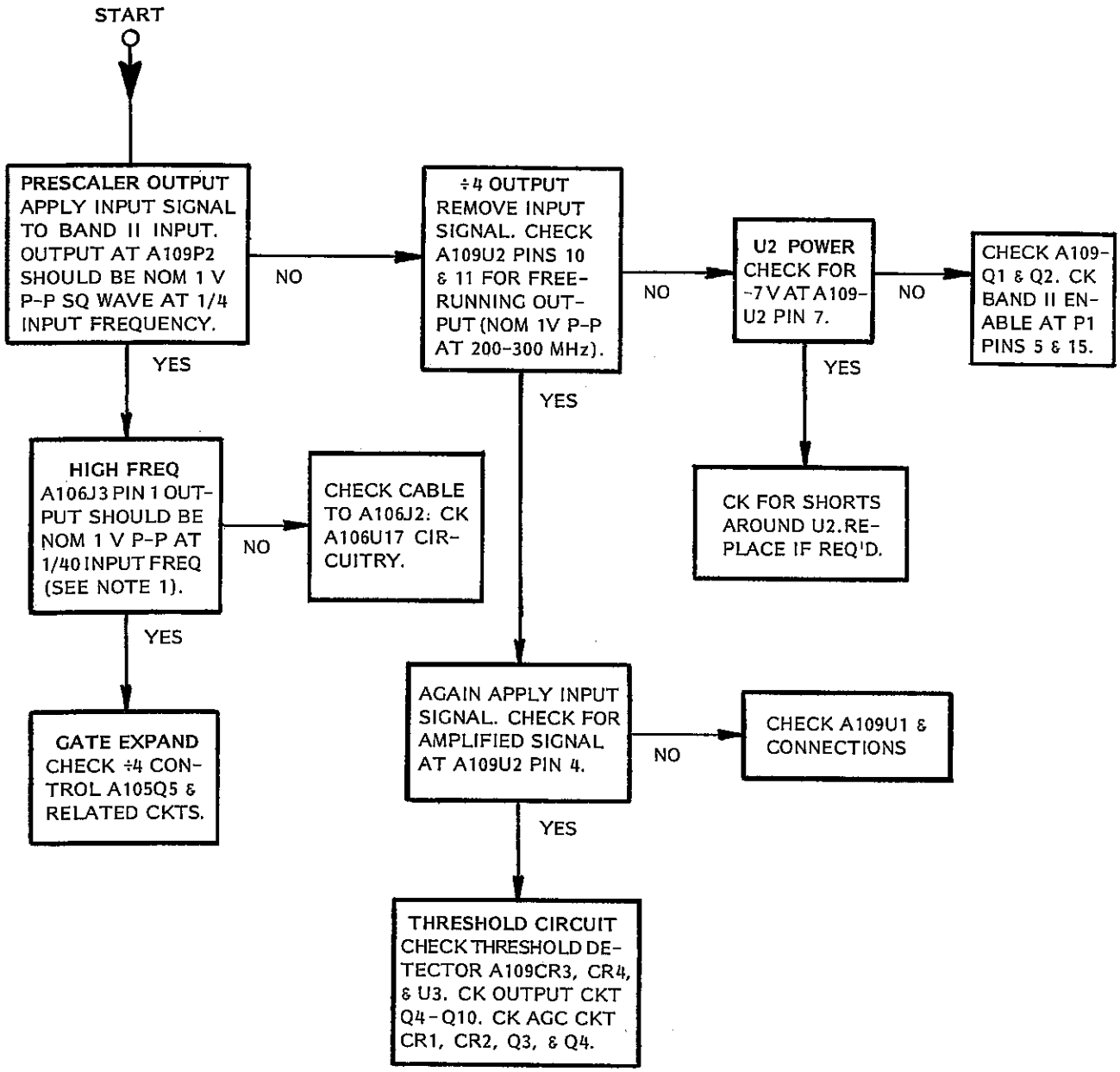


FIGURE 5-7
BAND IA
TROUBLESHOOTING TREE



NOTE 1: TROUBLESHOOTING OF A106 REQUIRES USE OF A SAMPLING OSCILLOSCOPE WITH A 1 GHz OR GREATER BANDWIDTH. CARE MUST BE EXERCISED TO LOAD CIRCUIT JUNCTION LIGHTLY. MAXIMUM PROBE CAPACITANCE: 1 PF. MINIMUM RESISTANCE: 500 OHMS.

FIGURE 5-8
BAND II
TROUBLESHOOTING TREE

START

PHASE LOCK
SET BAND SELECT TO 10-300 MHz POSITION. CONNECT A201J1 TO BAND I INPUT. DISPLAY SHOULD SHOW 200 000 000 +1 (200 MHz).

NO → CHECK ALL INPUTS TO A201. A201 FAULTY.

YES → CONVERTER LOCK
SET COUNTER TO BAND III. APPLY INPUT SIGNAL. SEARCH INDICATOR SHOULD GO OUT.

NO → RAMP
GROUND A203TP1. CONNECT SCOPE TO UNGROUNDED END OF A202R75. TRACE SHOULD BE SIMILAR TO FIGURE A.

YES → YIG PRESET
REMOVE CABLE TO A106J4. DISPLAYED FREQUENCY IS YIG PRESET, & SHOULD BE BELOW INPUT BY 25-275 MHz.

NO → CHECK A202 DAC 1 OUTPUTS, A102 3-MSD DCU's, CONNECTIONS, YIG OFFSET AND SLOPE CALIBRATION.

YES → CHECK YIG DELAY CALIBRATION AND A203U1. CHECK A106U17.

NO → ENABLE COMMANDS
CHECK A202P1 PIN E FOR TTL HIGH, PIN 5 FOR TTL LOW.

NO → CHECK A203 DAC 1 ENABLE AND CLOCK ENABLE

YES → CHECK A202 DAC CLOCK, DAC 1, & YIG DRIVER

YES → DETECTED LINES
REMOVE INPUT SIGNAL. SET SCOPE TO DC, 20 mV/DIV. MONITOR A204J3. COMB LINES SIMILAR TO FIG 6-3 SHOULD BE OBSERVED.

ALL LINES WEAK OR MISSING → MIXER CHECK
APPLY INPUT SIGNAL. SET SCOPE TO DC, 20 mV/DIV. RAISE INPUT LEVEL FROM -30 TO 0 dBm. OUTPUT LEVEL SHOULD INCREASE APPROX 100 mV.

NO → MIXER FAILURE VERIFICATION AND REPLACEMENT
TURN COUNTER OFF. REMOVE SCREWS HOLDING A204 TO CHASSIS. LOOSEN AND REMOVE COAX INPUTS TO MIXER. UNPLUG AND REMOVE A204. REMOVE SCREWS HOLDING MIXER TO A204. REMOVE MIXER. APPLY 0 dBm SIGNAL IN 1-18 GHz RANGE TO DIRECT INPUT (ATTENUATOR END). MONITOR DC OUTPUT (50-250 mV) WITH SCOPE AT IF CONNECTOR.

YES → MIXER OK. CHECK A204 DETECTOR/-AMPLIFIER CKT.

NO → REPLACE MIXER

YES → SOURCE/AMPLIFIER
TURN COUNTER OFF. REMOVE CABLE FROM A201J1. CONNECT J1 THROUGH A 30 dB, 1 WATT ATTENUATOR TO BROADBAND CALIBRATED DETECTOR. TURN COUNTER ON. CAUTION: 1 WATT AT 200 MHz AT A201J1. CONNECT SCOPE CHAN A (2 V/DIV) TO A201FL1, CHAN B TO DETECTOR OUTPUT. SET CHAN B SO FULL SCALE CORRESPONDS TO 0 dBm INTO DETECTOR (1 WATT AT A201J1). CHANNELS A & B SHOULD HAVE SIMILAR WAVEFORMS (SEE UPPER TRACE OF FIGURE 6-3), WITH MAXIMUM DETECTOR OUTPUT CORRESPONDING TO APPROXIMATELY 1 WATT AT A201J1.

NO → CHECK A201 (SOURCE/-AMPL) INPUT LINES. REPLACE A201.

YES → COMB GENERATOR
CHECK FOR +12 V AT A207 HEATER. CHECK OUTPUT COAX CABLE. REPLACE A207.

SOME LINES WEAK OR MISSING → RECALIBRATE PER PARAGRAPH 6-7d

YES → DETECTED INPUT
SET COUNTER TO BAND IA OR IB. SET SCOPE TO DC, 20 mV/DIV. MONITOR A204TP1; NOTE LEVEL. APPLY 1 GHz, 0 dBm, SQ WAVE TO INPUT. APPROX 100 mV SQ WAVE AT TP1.

NO → PIN ATTENUATOR TEST
CALIBRATE A206 PER PARAGRAPH 6-7d (1)-(5). IF SQUARE WAVE DOES NOT APPEAR, REMOVE CABLE TO A204J5. DOES SQUARE WAVE NOW APPEAR?

YES → CHECK A203 NOISE CONTROL CKT

NO → REMOVE SIGNAL. CHECK DCV AT A206P1 AND P2. P1 SHOULD BE APPROX -8V; P2 APPROX +7 V.

YES → REPLACE A206 (PIN ATTEN)

NO → REMOVE CABLE TO A204J3 AND J4. USING OHMMETER, CHECK A206P1 AND P2 AS FOLLOWS: P2 TO GND - DIODE (CATHODE GROUNDED), P1 TO GND - OPEN (BOTH POLARITIES), P1 TO P2 - DIODE (CATHODE TO P1), ARE ALL READINGS CORRECT?

YES → A204 ATTENUATOR DRIVER FAULTY

NO → REPLACE A206 (PIN ATTEN)

YES → VIDEO DETECTOR
GROUND A203TP1. APPLY INPUT SIGNAL. CONNECT SCOPE CHANNEL A TO UNGROUNDED END OF A202-R75 (RAMP), AND CHANNEL B TO A203TP6 (VIDEO DET). TRACE SHOULD MATCH FIGURE B.

NO → CHECK A203CR1 & U8 (VIDEO DET). IF OK, REPLACE A204, A205, A206 ASSY.

YES → MOVE GROUND FROM TP1 TO TP2. APPLY INPUT SIGNAL. OUTPUT SHOULD MATCH FIGURE 9-17C.

MISSING SIGNAL → TROUBLESHOOT A203

ALL SIGNALS PRESENT → CHECK A202 DAC 2. RECALIBRATE PER SECTION 6.

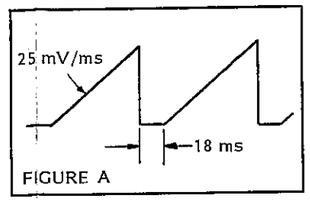


FIGURE A

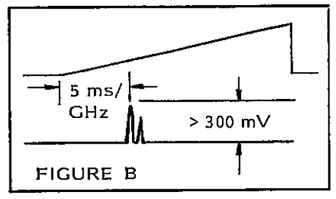


FIGURE B

FIGURE 5-9
BAND III
TROUBLESHOOTING TREE

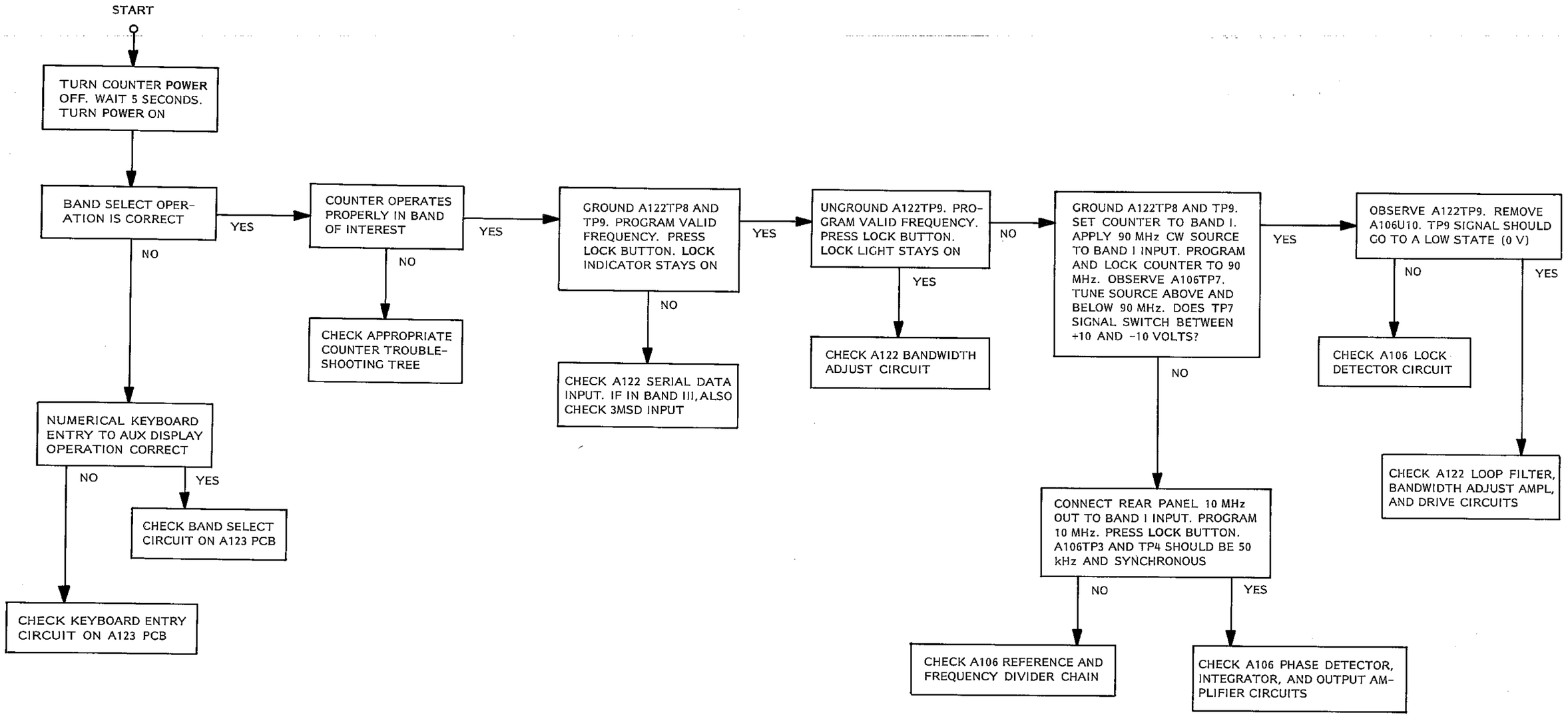


FIGURE 5-10
LOCKBOX OPERATION
TROUBLESHOOTING TREE

SECTION 6

ADJUSTMENTS & CALIBRATION

6-1. GENERAL

6-2. This section describes the procedures to be followed to correctly adjust the EIP Counter. In general, adjustments should be made only if the instrument is not operating within specifications, or following replacement of components. Test equipment required is specified in Table 5-1. If adjustments do not result in the specified performance, refer to Section 5.

> **IMPORTANT**
>
> Many adjustments are dependent upon previous ones. It is essential that care be taken to perform adjustments in exactly the order presented below. Adjustment locations are shown in Figure 6-1.

6-3. POWER SUPPLY ADJUSTMENT

6-4. Prior to any power supply adjustments, the instrument should be allowed to warm-up for at least 20 minutes. All voltages are measured on Counter Interconnect board A113. Adjustments are made according to the following procedure:

a. Connect DVM to GND on A113.

b. Measure +12 VDC output. Adjust A107R7 until output is +12.000 ± .010 VDC.

c. Measure +5 VDC output. Adjust A107R15 until output is +5.000 ± .010 VDC.

d. Measure -12 VDC output. Adjust A107R21 until output is -12.000 ± .010 VDC.

e. Measure -5.2 VDC output. Adjust A107R31 until output is -5.200 ± .010 VDC.

6-5. BAND I ADJUSTMENTS (20 Hz to 300 MHz)

No Band I adjustments are required.

6-6. BAND II ADJUSTMENTS (100 MHz to 850 MHz)

a. Threshold:

(1) Set counter to the Band II (100 MHz - 850 MHz) position.

(2) Connect a 100 MHz, -15 dBm CW signal to the Band II input connector. Set A109R41 (on Prescaler) to maximum sensitivity.

(3) Reduce signal level until counter just begins to miscount.

(4) Adjust A109R41 until the reading just drops to all zeros.

6-7. BAND III ADJUSTMENTS (825 MHz to 18 GHz)

a. For all the following tests, set counter to the Band III (825 MHz - 18 GHz) position.

b. Video Detector Gain (see also Paragraph 6-7g.):

(1) Disconnect cable from output of Video Amplifier (A204J2).

(2) Connect a 150 MHz CW signal at -6 dBm to Cable A203P2 (W21).

(3) Connect DVM to Converter Control 1 Test Point A203TP6.

(4) Adjust A203R22 for 300 ± 20 millivolts.

c. In-Band Detector switching point:

(1) Connect sweep generator to A203P2. Set controls as follows:

Sweep	265 MHz downward to 245 MHz
Level	0 dBm
Markers	Every 10 MHz

(2) Connect dual trace oscilloscope as follows:

Horizontal	To sweep generator
Ch. A	A203TP4 via vertical output on sweep generator.

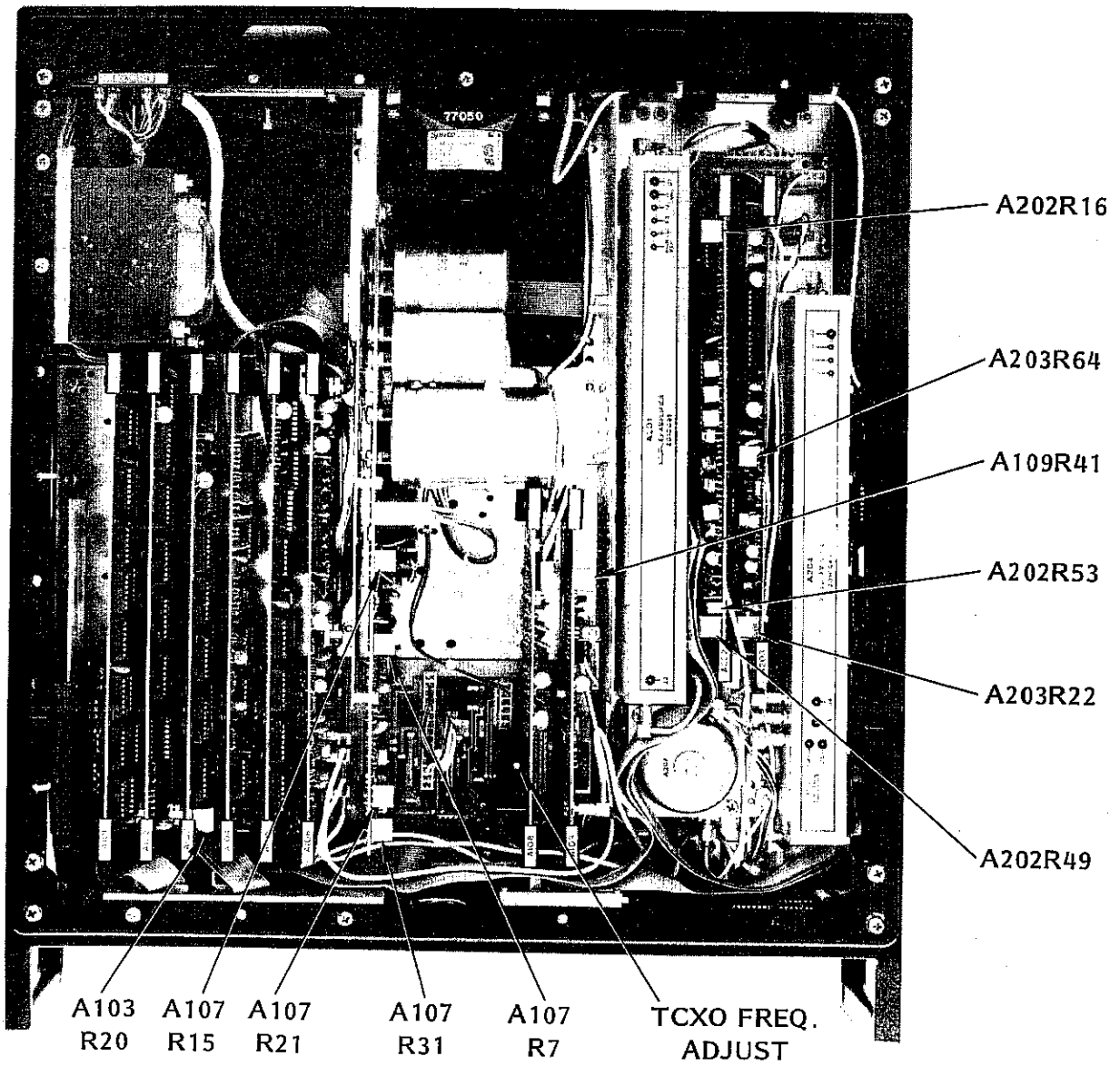


FIGURE 6-1
CALIBRATION
ADJUSTMENT
LOCATOR

(3) Adjust A203R64 so the switching spike is coincident with the 250 MHz marker as shown in Figure 6-2.

(4) Reconnect cable to A204J2.

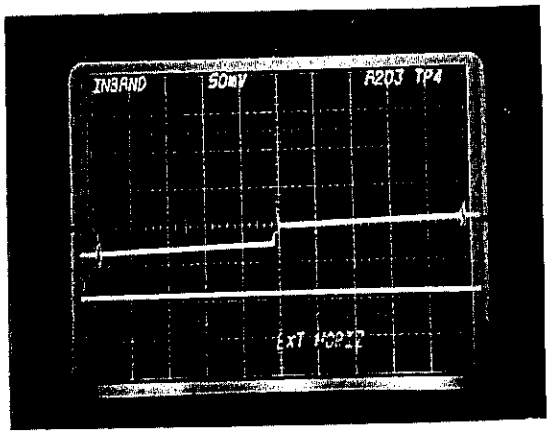


FIGURE 6-2
IN-BAND DETECTOR SWITCHING POINT

d. PIN Level Control Threshold:

(1) Unplug Source/Amplifier power plug A208J1.

(2) Connect a 3 dB pad to the Band III input connector. Apply a +3 dBm, 1.0 GHz, square-wave modulated signal to the pad.

(3) Observe the square-wave signal at A204TP1.

(4) Adjust A204R61 until the square-wave at TP1 is 90 to 100 mV in amplitude.

(5) Reconnect Source/Amplifier power plug.

e. YIG Driver Offset and Slope:

NOTE: For this adjustment a Summing Amplifier capable of providing a variable DC offset is recommended. One can be constructed as shown in Figure 5-1, or a dual trace oscilloscope with differential inputs (such as HP1200A) may be used if the signal is applied to one side of the differential input, and a variable DC power supply to the other input.

(1) Connect dual trace oscilloscope as follows:

Ch. A	A203TP6 (Video Detector Output)
Ch. B	A202J3 pin 1 (Ramp) via Summing Amplifier
Ext. Trig.	A203TP5 (CONVERTER RESET)

(2) Ground A203TP1.

(3) Apply a signal of approximately 1.1 GHz at -15 dBm to Band III input.

(4) Depress RESET switch.

(5) With no DC offset applied, adjust Channel B vertical sensitivity so each ramp step is two vertical divisions (approximately 10 mV/div). Set Channel A to 20 mV/div. Set time base to 5 ms/cm and set time base multiplier to X10. Oscilloscope display should appear as shown in Figure 6-3.

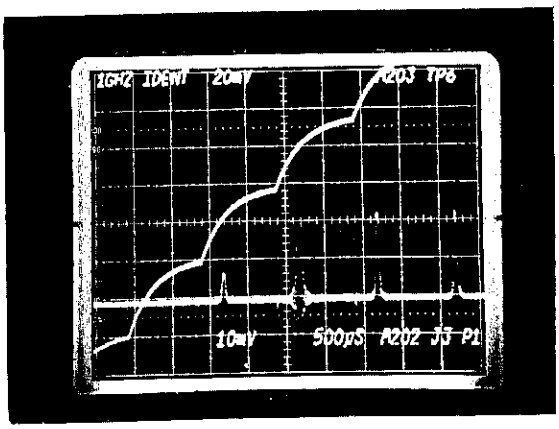


FIGURE 6-3
1 GHz COMB LINE IDENTIFICATION

(6) Reduce the input frequency to 1.0 GHz. When the input frequency is exactly 1 GHz, the center line of the three comb lines on Channel A should null. This identifies the 1 GHz comb line. The 800 MHz comb line is the line preceeding the 1 GHz line.

(7) Remove the ground from A203TP1 and place it on A203TP2. Depress the RESET switch.

(8) Adjust YIG Offset A202R49 so the ramp resets at 50% (1 div) of the fourth ramp step (See Figure 6-4).

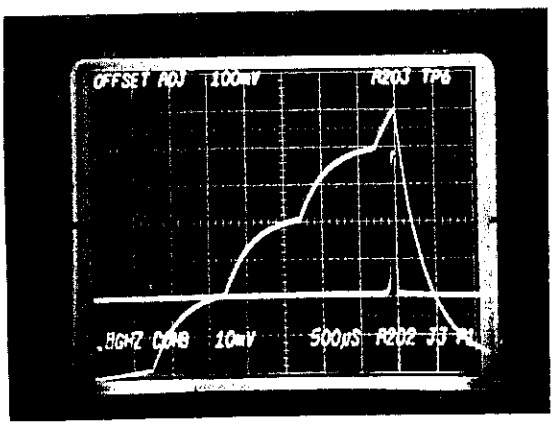


FIGURE 6-4
YIG DRIVER OFFSET ADJUSTMENT

(9) Tune slowly from 1 GHz to 18 GHz. As the frequency is changed, adjust the DC offset and the horizontal position control of the oscilloscope to maintain the upper portion of the ramp on the display. Above 10 GHz, the time base will need to be increased to 10 msec/div.

As the frequency is changed, adjust YIG slope with A202R53, so the ramp reset occurs in the range of 40 to 60% of the full step amplitude. At 18 GHz, adjust R53 so reset occurs at 60% of the step amplitude.

(10) Recheck YIG Offset A202R49 and readjust at 1 GHz if necessary. If A202R49 is readjusted, it will be necessary to reset YIG Slope A202R53 at 18 GHz.

f. YIG Delay Correction

(1) With connections as in paragraph 6.7e, set input frequency to 1 GHz at -15 dBm, and oscilloscope time base control to 10 ms/div., unexpanded.

(2) Adjust YIG Delay Correction A202R16 so display appears approximately as shown in Figure 6-5.

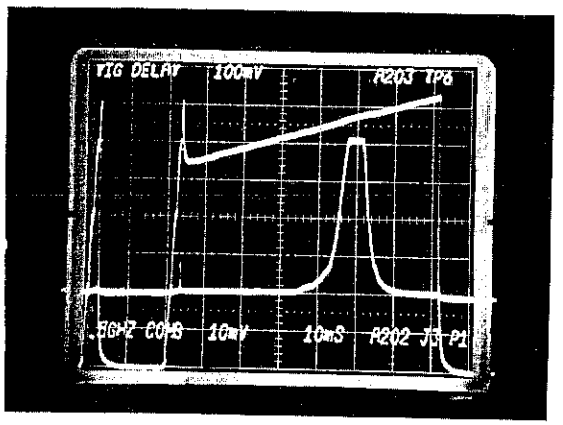


FIGURE 6-5
YIG DELAY CORRECTION 1

(3) Set time base to variable (approx. 5 ms/div) and externally trigger oscilloscope from A203P1 pin 12 (DAC 2 ENABLE). Adjust oscilloscope time base so DAC 2 ramp occupies the full screen.

(4) Adjust A202R16 so the 50% point of the leading edge of the video pulse occurs one division to the right of center of the DAC 2 ramp as shown in Figure 6-6. Note that the point marked "Ramp Start" is 3 ms after DAC 2 ENABLE, and that the point marked "Ramp Center" is *not* the center of of the display.

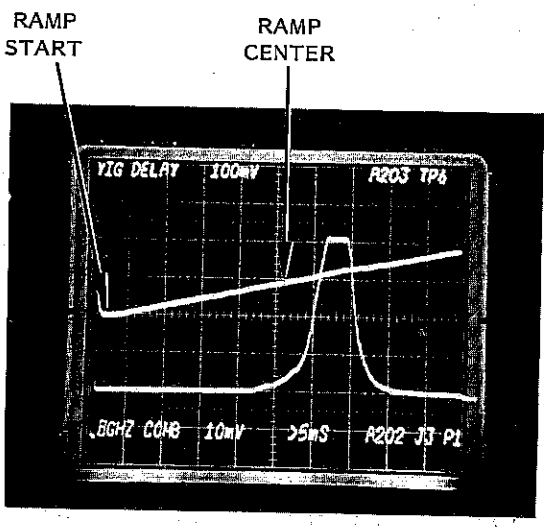


FIGURE 6-6
YIG DELAY CORRECTION 2

(5) Tune to 18 GHz and observe the position of the leading edge with respect to DAC 2 "Ramp Center". This should be approximately one division to the left of "Ramp Center".

(6) If necessary readjust A202R16 until the leading edge of the video pulse is the same distance to the right of "Ramp Center" at 1 GHz, as it is to the left of "Ramp Center" at 18 GHz.

g. Final Video Detector Gain Adjustment

NOTE: The procedure given in paragraph 6-7b will not result in optimum performance. The following procedure sets the Video Detector gain to give maximum sensitivity without loss of instrument accuracy.

(1) Set the source power level to -20 dBm, and frequency to 8 GHz. Connect source to the Band III input.

(2) Using the phase locking capability of the 371, lock the source to 8 GHz.

(3) Reduce input power slowly. At some power level, counter will lose lock.

(4) Increase power slightly so counter will just achieve lock and a frequency is displayed. Phase lock the source again.

(5) Displayed frequency should be correct (no reduction in indicated frequency). Increase Video Detector gain (adjust A203R22), and repeat steps (3) and (4) until an erroneous count is obtained.

(6) Once an erroneous count is obtained, begin decreasing Video Detector gain and repeat steps (3) and (4) until frequency indication is either correct, or zero (no LOCK), as power level is varied and counter is reset.

h. Comb Leveling/Bias:

NOTE: The most important function of comb leveling is to insure that spurious mixing products (due to doubling of the comb frequency within the Mixer), do not cause erroneous readings. Thus this leveling procedure insures that maximum output due to these mixing products are below the lock threshold.

(1) Connect oscilloscope as follows:

Ch. A	A203TP6 (Video Detector output)
Ext. Trig.	A202P1 pin 12 (CONV. RESET)
Time Base	2 ms/div

(2) Ground A203TP1.

(3) Apply a 1.5 GHz signal at +7 dBm; observe the Video Detector signal.

(4) Slowly tune the frequency upward. At some frequencies, a spurious output corresponding to approximately one half the input frequency will be visible.

(5) As the frequency is varied from 1.5 to 18 GHz, adjust A202R69 so no spurious signal has an amplitude in excess of 290 mV. Refer to Figure 6-7 for a typical display. (Vary scope time base as necessary to keep the display on the screen.)

IMPORTANT: Do not attenuate comb lines more than absolutely necessary to maintain maximum spurious outputs of 290 mV. Comb line power relates directly to sensitivity.

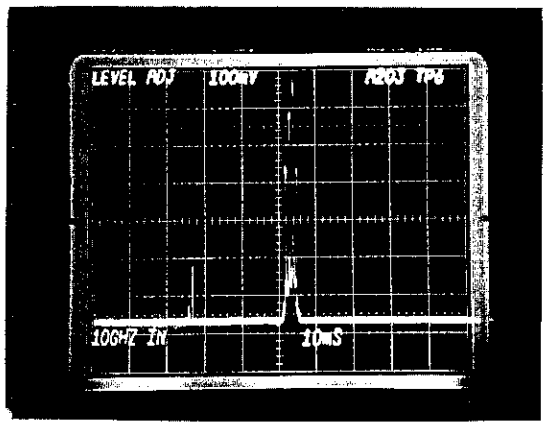


FIGURE 6-7
COMB FREQUENCY HARMONIC GENERATION

6-8. TIME BASE CALIBRATION

IMPORTANT

The precision of time base calibration directly affects overall counter accuracy. Reasons for recalibration, and procedures to be used, should be thoroughly understood before attempting any readjustment.

6-9. The fractional frequency error in the frequency indicated by the counter, is equal to the negative of the fractional frequency error of the Time Base Oscillator with respect to its true value. That is:

$$\frac{\Delta f_s}{f_s} = -\frac{\Delta f_t}{f_t}$$

where f_s is the true frequency of the measured signal, and f_t is the true frequency of the Time Base Oscillator. Thus the inaccuracy associated with a frequency measurement, is directly related to the quality of the Time Base Oscillator, and a measure of the precision with which it was originally adjusted.

6-10. TCXO CALIBRATION

6-11. The standard time base oscillator used in the counter is a temperature-compensated crystal oscillator: a TCXO (A116). The highest and lowest actual measured frequencies of this oscillator will differ by no more than 2 parts in 10^6 if the temperature is varied slowly from 0° to +50°C. Therefore, an indicated measurement will exhibit the same fluctuation even though the signal being measured is not changing. To center this fluctuation on the true value of the measured signal, each TCXO has imprinted on its side, the frequency to which it must be set at +25°C. The calibration procedure for this adjustment is described in Paragraphs 6-15 through 6-17.

6-12. At approximate room temperature (+25°C.), the slope of the frequency vs. temperature curve, is normally no worse than -1×10^{-7} parts per °C. Therefore, if the counter is used in an ordinary laboratory environment, the TCXO may be set as close to 10 000 000 Hz as desired. In this environment, a peak-to-peak temperature variation of 5°C. will result in a measured signal error due to oscillator temperature characteristics of no more than $\pm 2.5 \times 10^{-7}$ parts. Refer to Paragraphs 6-23 through 6-26 for a recommended adjustment procedure.

6-13. Another source of inaccuracy in the measured signal due to the Time Base Oscillator originates in the natural aging characteristic of the crystal. Aging refers to the long term, irreversible change in frequency, generally in the positive direction, which all quartz oscillators

experience. The magnitude of this frequency fluctuation in the TCXO is specified to be less than 3×10^{-7} parts per month. This may be expected to improve in time to be no worse than 1×10^{-8} parts per year in continuous service.

6-14. Error due to aging adds directly to error due to temperature perturbations. Thus the frequency of recalibration is dependent upon the overall accuracy requirement of the counter and its environment. For example: If the counter is subjected to the full operating temperature range, and initially adjusted properly, then one month later, the inaccuracy over temperature could be expected to vary from $+ 1.3 \times 10^{-6}$ parts, to $- 0.7 \times 10^{-6}$ parts.

6-15. TCXO CALIBRATION PROCEDURE

NOTICE

For both TCXO recalibration methods: Remove top cover of counter. Connect counter to reliable power source. Note ambient temperature.

6-16. METHOD 1:

a. Measure the frequency of the TCXO at the rear panel 10 MHz IN/OUT connector, with a second counter of known calibration accuracy.

b. Adjust the TCXO if necessary, by turning the calibration screw on the TCXO case until the measured frequency is the same as that shown on the TCXO calibration label.

6-17. METHOD 2:

a. Apply a 10 000 000 Hz signal from a frequency standard or other oscillator of suitable accuracy and stability to the Band I input of the counter. All RESOLUTION switches should be set to display all the digits including the 1 Hz digit.

b. Adjust the TCXO until the indicated reading on the counter is offset from 10 000 000 Hz by the negative of the frequency shown on the TCXO. For example: If the TCXO calibration label shows a frequency of 10 000 003 Hz, adjust the TCXO until the displayed reading shows 9 999 997 Hz.

6-18. OVEN STABILIZED OSCILLATOR CALIBRATION

6-19. If one of the Oven Stabilized Oscillator options is installed in the counter (see Section O), the effects of temperature perturbations and aging must still be considered, although the magnitude of these inaccuracies associated with each oscillator are greatly reduced.

6-20. Full benefit of the Oven Stabilized Oscillator characteristics can only be realized if the Oscillator is running continuously: that is, with the counter always connected to a source of AC power. Under these conditions, the perturbations in frequency will generally be in the positive direction for either an increase or decrease in temperature from +25°C. The aging characteristic is also generally in the positive direction.

6-21. The frequency of readjustment of the Oven Stabilized Oscillator is determined by the level of accuracy required. A method of adjusting the oscillator to an inaccuracy of less than 1×10^{-9} parts, relative to a standard, is given in Paragraphs 6-22 through 6-26.

6-22. OVEN STABILIZED OSCILLATOR TEST PROCEDURE

NOTE: This procedure is also usable with the TCXO under the conditions described in Paragraph 6-12.

6-23. TEST EQUIPMENT REQUIRED:

See Table 5-1.

6-24. Figure 6-8 shows the test set-up for determining the frequency of the Oven Stabilized Oscillator (A112). The frequency inaccuracy, relative to a standard, is determined by observing the drift of the oscilloscope pattern. The fractional frequency offset is computed from:

$$\frac{T_{\text{drift of zero crossing}}}{T_{\text{observation time of drift}}} = \frac{\Delta f}{f}$$

For example: If the pattern drifts at a rate of .01 microsecond every 10 seconds, the frequency is in error by 1 part in 10^9.

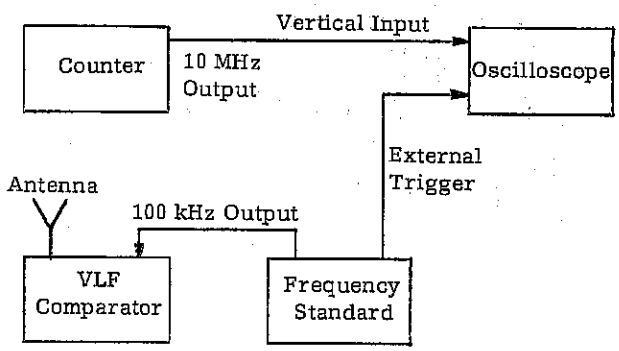


FIGURE 6-8
TIME BASE CALIBRATION

6-25. All frequency checks and adjustments should be made only after the Oven Stabilized Oscillator has been connected to its operating power supply for 24 hours. If the oscillator has been disconnected from its power source for more than 24 hours, it may require 72 hours of continuous operation to achieve the specified frequency aging rate (refer to paragraph 7-12).

6-26. TO MEASURE OSCILLATOR FREQUENCY:

a. Connect the counter's internal oscillator output signal from the 10 MHz IN/OUT connector (on the rear panel of the counter) to the vertical input of the oscilloscope.

b. Trigger oscilloscope externally with the frequency standard. The VLF Comparator is used to determine the absolute frequency of the standard.

c. Set oscilloscope sweep rate to 0.1 μ sec/cm and expand X10; this results in a sweep rate of .01 μ sec/cm.

d. Adjust oscilloscope vertical controls for maximum gain.

e. Determine the frequency difference (see para. 6-24).

f. Horizontal drift of oscilloscope display in μ sec/sec, is a measure of the difference between the frequency standard and the counter oscillator frequency. If the difference is excessive for the desired counter application, vary the TIME BASE ADJUST control on the rear panel of the counter until the pattern stops drifting. NOTE: For highest accuracy, the counter should be operated for 72 hours prior to adjustment.

6-27. LOCKBOX ADJUSTMENTS

No lockbox adjustments are required.

6-28. Instrument calibration is now complete.

SECTION 7

PERFORMANCE TESTS

7-1. GENERAL

7-2. The purpose of this section is to enable the user to verify that the counter meets specifications over the entire frequency range.

7-3. VARIABLE LINE VOLTAGE

7-4. During the performance tests the counter should be connected to the power source through a variable voltage device so that line voltage may be varied ± 10% from nominal (115 or 230 Vac) to assure proper operation of the counter under various supply conditions.

7-5. RECOMMENDED TEST EQUIPMENT

7-6. See Table 5-1 for recommended test equipment. Other equipment may be used provided that performance is equal to, or better than, that listed in the table.

7-7. PERFORMANCE TESTS

7-8. RANGE AND SENSITIVITY — BAND IA (20 Hz to 135 MHz)

a. Set controls as follows:

(1) SAMPLE RATE: Fully counter-clockwise.

(2) BAND SELECT: 20 Hz - 135 MHz range.

(3) TIME BASE switch: Set to INT.

b. Connect signal source output to Band I input via 50 ohm shunt feedthru resistor (to terminate source).

c. Set signal level to 25 mV rms (-19 dBm into 50 ohms).

d. Vary signal from 20 Hz to 135 MHz (changing signal source as required). Counter should display correct input frequency.

7-9. RANGE AND SENSITIVITY — BAND IB (10 MHz to 300 MHz)

a. Set controls as follows:

(1) SAMPLE RATE: Fully counter-clockwise.

(2) BAND SELECT: 10 MHz - 300 MHz range.

(3) TIME BASE switch: Set to INT.

b. Connect signal source output to Band I input.

c. Vary signal frequency from 10 MHz to 300 MHz at -20 dBm (22 mV rms) power level. Counter should display correct input frequency.

7-10. RANGE AND SENSITIVITY — BAND II (100 MHz to 850 MHz)

a. Set controls as follows:

(1) SAMPLE RATE: Fully counter-clockwise.

(2) BAND SELECT: 100 MHz - 850 MHz range.

(3) TIME BASE switch: Set to INT.

b. Connect signal source output to Band II input.

c. Vary signal frequency from 100 MHz to 150 MHz at -15 dBm (40 mV rms) power level. Counter should display correct input frequency.

d. Change level to -20 dBm (22 mV rms). Vary frequency from 150 MHz to 850 MHz. Counter should display correct frequency.

7-11. RANGE AND SENSITIVITY — BAND III (825 MHz to 18 GHz)

a. Set controls as follows:

(1) SAMPLE RATE: Fully counter-clockwise.

(2) BAND SELECT: 825 MHz - 18 GHz range.

(3) TIME BASE switch: Set to INT.

b. Connect leveled source output to Band III input.

c. Vary signal frequency from 825 MHz to 18 GHz at the following levels:

825 MHz - 1.1 GHz	-25 dBm (12 mV rms)
1.1 GHz - 12.4 GHz	-30 dBm (7 mV rms)
12.4 GHz - 18.0 GHz	-25 dBm (12 mV rms)

Counter should display correct input frequency.

FSCM	MFR NAME,ADDRESS,ZIPCODE
01121	ALLEN-BRADLEY CO.,SO.MILWAUKEE,WI 53204
01295	TEXAS INSTRUMENTS INC.,DALLAS,TX 75222
02660	AMPHENOL CONNECTOR DIV.,BUNKER RANO CORP.,BROADVIEW,IL 60153
04618	AMERICAN PAMCOR INC.,PAOLI,PA 19301
04713	SEMICONDUCTOR DIV.,MOTOROLA INC.,PHOENIX,AZ 85008
05591	GENERAL RESISTANCE DIV.,CHRONETICS INC.,MT.VERNON,NY 10550
06665	PRECISION MONOLITHICS,SANTA CLARA,CA 95050
07263	FAIRCHILD SEMICONDUCTOR, MOUNTAIN VIEW,CA 94040
09353	C AND K COMPONENTS INC.,WATERTOWN,MA 02172
11236	CTS OF BERNE INC.,BERNE,IN 46711
11532	TELEDYNE RELAYS,HAWTHORNE,CA 90250
12436	GENERAL DYNAMICS CORP.,SAN DIEGO,CA 92112
14099	SEMTECH CORP.,NEWBURY PARK,CA 91320
14298	AMERICAN COMPONENTS INC.,CONSHOHOCKEN,PA 19428
14433	ITT SEMICONDUCTOR DIV.OF ITT CORP.,W.PALM BEACH,FL 33401
20764	KMC SEMICONDUCTOR CORP.,LONG VALLEY,NJ 07853
21793	DANA LABORATORIES INC.,IRVINE,CA 92664
23880	STANFORD APPLIED ENGINEERING INC.,SANTA CLARA,CA 95050
23936	PAMOTOR INC.,BURLINGAME,CA 94010
26654	VARADYNE INDUSTRIES,SANTA MONICA,CA 90404
28480	HEWLETT-PACKARD CO.,PALO ALTO,CA 94304
32293	INTERSIL INC.,CUPERTINO,CA 95014
34649	INTEL CORP,SANTA CLARA,CA 95051
50522	ELECTRONIC SPECIAL PRODUCTS,MONSANTO CO.,CUPERTINO,CA 95014
50579	LITRONIX INC.,CUPERTINO,CA 95014
56289	SPRAGUE ELECTRIC CO.,NORTH ADAMS,MA 01247
70903	BELDEN CORP.,CHICAGO,IL 60644
71279	CAMBRIDGE THERMIONIC CORP.,CAMBRIDGE,MA 02138
71400	BUSSMAN MFG DIV.,MCGRAW-EDISON CO.,ST.LOUIS,MO 63107
71590	CENTRALAB DIV,GLOBE-UNION INC.,MILWAUKEE,WI 53201
71785	CINCH DIV.,TRW ELECTRONIC COMPONENTS,ELK GROVE VILLAGE,IL 60007
72136	ELECTRO-MOTIVE MFG. CO.,WILLIMANTIC,CT 06226
72259	NYTRONICS INC.,PELHAM MANOR,NY 10803
72982	ERIE TECHNOLOGICAL PRODUCTS INC.,ERIE,PA 16512
73138	HELIPOT DIV.,BECKMAN INSTRUMENTS,FULLERTON,CA 92634
75915	LITTELFUSE INC.,DES PLAINES,IL 60016
76854	OAK MFG DIV.,OAK ELECTRO/NETICS CORP.,CRYSTAL LAKE,IL 60014
80031	MEPCO/ELECTRA INC.,MORRISTOWN,NJ 07960
80294	INSTRUMENT DIV.,BOURNS INC.,RIVERSIDE,CA 92506
81349	MILITARY SPECIFICATION
82389	SWITCHCRAFT INC.,CHICAGO,IL 60630
86797	ROGAN BROS.INC.,SKOKIE,IL 60076
88140	CUTLER-HAMMER INC.,LINCOLN,IL 62656
91637	DALE ELECTRONICS INC.,COLUMBUS,NE 68601
91836	KINGS ELECTRONICS CO.,TUCKAHOE,NY 10707
95275	VITRAMON INC.,BRIDGEPORT,CT 06601
96341	MICROWAVE ASSOCIATES,BURLINGTON,MA 01801
98291	SEALECTRO,MAMARONECK,NY 10544
99800	DELAVAN DIV.,AMERICAN PRECISION INDUST.,EAST AURORA,NY 14052
	FOLLOWING MFRS DO NOT HAVE FSCM NUMBER
0000A	MOLEX INC.,LISLE,IL 60532
0000B	STETTNER-TRUSH,CAZENOVIA,NY 13035
0000C	PLESSEY ELECTRO-PRODUCTS,LOS ANGELES,CA 90066
0000L	R-OHM CORPORATION,IRVINE,CA 92664
0000S	CALIFORNIA EASTERN LABS.,BURLINGAME,CA 94010
0000T	DATA DISPLAY PRODUCTS,LOS ANGELES,CA 90009
0000X	ANY MANUFACTURER OF THIS PRODUCT

TABLE 8-2. LIST OF MANUFACTURERS

EIP P/N	ITEM DESCRIPTION	MFR	MFR PART NUMBER
2010061	ASSY:FRNT END,CONVERTER	EIP	(PN D10)
2020109	PCB ASSY:KEYBOARD	EIP	371
2030010-01	OSC,OVENIZED:5X10-9	EIP	
2030010-02	OSC,OVENIZED:1X10-9	EIP	
2030010-03	OSC,OVENIZED:5X10-10	EIP	
2040014	ASSY:HARNESS	EIP	
2040152	ASSY:CABLE,FLEX,CO-AX	EIP	371(W34)
2100002	CAP:CHIP .001UF 20% 50V	95275	VJ1210A102MF
2100005	CAP:CHIP 150PF 100V	26654	38N100S151K
2150001	CAP:CER .001UF 20% 1KV	56289	5GA-D10
2150003	CAP:CER .01UF 20% 100V	56289	TG-S10
2150005	CAP:CER .002UF 20% 1KV	56289	5GA-D20
2150006	CAP:CER .02UF 20% 100V	56289	TG-S20
2150008	CAP:CER .005UF 20% 100V	56289	TG-D50
2150009	CAP:CER .05UF 20% 100V	56289	TG-S50
2150010	CAP:CER .05UF 20V	71590	UK20-503
2150999	CAP:CER-SELECT AT TEST	56289	TG-XXX
2160002	CAP:CER 1.0PF NPO 500V	72982	301000C0KQ109C
2160004	CAP:CER 10PF NPO 500V	72982	301000C0HQ100C
2160005	CAP:CER 12PF NPO 500V	72982	301000C0GQ120C
2160006	CAP:CER 15PF NPO 500V	72982	301000C0GQ150J
2160007	CAP:CER 18PF NPO 500V	72982	301000C0GQ180J
2160008	CAP:CER 2.2PF NPO 500V	72982	301000C0JQ229C
2160010	CAP:CER 24PF NPO 500V	72982	301000C0GQ240J
2160013	CAP:CER 4.7PF NPO 500V	72982	301000C0HQ479C
2160015	CAP:CER 8.2PF NPO 500V	72982	301000C0HQ829C
2160016	CAP:CER 20PF NPO 500V	72982	301000C0GQ200J
2160999	CAP:CER-SELECT AT TEST	72982	301000C0XQXXXX
2200001	CAP:ELEC 1250UF 50V	80031	39CS50GL125I
2200010	CAP:ELEC 6500UF 25V	80031	91S25HA852
2200011	CAP:ELEC 40000UF 15V	80031	91S15JB44
2200012	CAP:ELEC 11000UF 15V	80031	39CS15JP113
2250001	CAP:MICA 10PF 5% 500V	72136	DM15CD100D0
2250002	CAP:MICA 100PF 5% 500V	72136	DM15CD101J0
2250003	CAP:MICA 1000PF 5% 500V	72136	DM15CD102J0
2250005	CAP:MICA 150PF 5% 500V	72136	DM15CD151J0
2250006	CAP:MICA 180PF 5% 500V	72136	DM15CD181J0
2250007	CAP:MICA 2.0PF25% 500V	72136	DM15CD2R0D0
2250008	CAP:MICA 20PF 5% 500V	72136	DM15CD200J0
2250009	CAP:MICA 200PF 5% 500V	72136	DM15CD201J0
2250011	CAP:MICA 220PF 5% 500V	72136	DM15CD221J0
2250012	CAP:MICA 27PF 5% 500V	72136	DM15CD270J0
2250014	CAP:MICA 33PF 5% 500V	72136	DM15CD330J0
2250017	CAP:MICA 47PF 5% 500V	72136	DM15CD470J0
2250018	CAP:MICA 470PF 5% 500V	72136	DM15CD471J0
2250021	CAP:MICA 56PF 5% 500V	72136	DM15CD560J0
2250025	CAP:MICA 68PF 5% 500V	72136	DM15CD680J0
2250026	CAP:MICA 680PF 5% 500V	72136	DM15CD681J0
2250031	CAP:MICA 7.0PF10% 500V	72136	DM15CD7R0K0
2250999	CAP:MICA-SELECT AT TEST	72136	DM15CDXXXX0
2260001	CAP:MICA 150PF 5% 500V	72136	DM10CD151J0
2300003	CAP:TANT .15UF 35V	14433	TAG20-0.15/35-50
2300005	CAP:TANT .47UF 35V	14433	TAG20-0.47/35-50
2300008	CAP:TANT 1.0UF 35V	14433	TAG20-1.0/35-50
2300010	CAP:TANT 10UF 16V	14433	TAG20-10/16-50
2300015	CAP:TANT 33UF 10V	14433	TAG20-33/10-50
2300017	CAP:TANT 47UF 6.3V	14433	TAG20-47/6.3-50
2300020	CAP:TANT .10UF 35V	14433	TAG20-.10/35-50
2300021	CAP:TANT 4.7UF 20% 16V	14433	TAG20-4.7/16
2300022	CAP:TANT 22UF 20% 20V	14433	TAG20-22/20-20
2300023	CAP:TANT 33UF 20% 20V	14433	TAG20-33/20
2300024	CAP:TANT 100UF 20% 6.3V	14433	TAG20-100/6.3
2300025	CAP:TANT 47UF 20% 16V	14433	TAG20-47/16-20
2350001	CAP:TRIM 2-8PF 250V	00008	10S-T-22-2/8
2350002	CAP:TRIM 5.5-18PF 250V	00008	10S-T-22-5.5/18
2350003	CAP:TRIM 8-25PF 250V	00008	10S-T-22-8/25
2350017	CAP,FDTH:RF FILTER,5KPF	04618	859556-1
2350022	CAP:TRIM 5.5-18PF 250V	00008	10S-T-24-5.5/18
2350024	CAP:FLM .039UF 10% 100V	56289	225P39391WD3
2610010	CONN:JACK,BLKHD,RECPT	98291	51-045-0000
2610017	CONN:PLUG,PC RCPT,STR	98291	52-052-0000
2610018	CONN:JACK,PC RCPT,STR	98291	51-051-0000
2610024	CONN:BNC,BLKHD,TRS FNSH	91836	KC-79-35
2620006	CONN:PC WAFER 6PIN ML	0000A	09-18-5061
2620012	CONN:PC WAFER 9PIN, ML	0000A	09-18-5091
2620014	CONN:PC WAFER 4PIN, ML	0000A	09-60-1041
2620016	CONN:PC WAFER, 6PIN, ML	0000A	09-60-1061
2620018	CONN:PC EDGE 18PIN	04618	1-583407-8
2620019	CONN:PC EDGE 8PIN	04618	583407-9
2620027	JACK:PC .080 PIN FML	71279	3398-01-03
2620029	CONN:PC RT AN,3PIN, ML	0000A	09-66-1031
2620030	CONN:PC RT AN,4PIN, ML	0000A	09-66-1041
2620031	CONN:PC RT AN,7PIN, ML	0000A	09-66-1071
2620042	CONN:PC WAFER, 9PIN, ML	0000A	09-60-1091
2620044	CONN:PC WAFER,12PIN, ML	0000A	09-60-1121
2620047	CONN:PC WAFER, 5PIN, ML	0000A	09-60-1051
2630002	SOCKET: 16 PIN,NYLON	0000A	A-4497-16
2630003	SOCKET: 14 PIN,NYLON	0000A	A-4497-14
2630009	SOCKET: 14 PIN IC	71785	14-N-DIP
2630010	SOCKET: 16 PIN IC	71785	16-N-DIP

TABLE 8-3. MASTER PARTS LIST

EIP P/N	ITEM DESCRIPTION	MFR	MFR PART NUMBER
2640004	CONN 50PIN	02660	57-40500
2640005	RECEPTACLE	82389	EAC-301
2700827	DIODE: 6.2V ZENER	04713	1N827
2704001	DIODE: RECT	04713	1N4001
2704154	DIODE: GEN PURP	07263	1N4154
2704370	DIODE: 2.4V ZENER	04713	1N4370
2704757	DIODE: 51V ZENER	04713	1N4757
2705225	DIODE: 3.0V ZENER	0000X	1N5225
2705227	DIODE: 3.6V ZENER	04713	1N5227
2705230	DIODE: 4.7V ZENER	04713	1N5230
2705231	DIODE: 5.1V ZENER	04713	1N5231
2705234	DIODE: 6.2V ZENER	04713	1N5234
2705237	DIODE: 8.2V ZENER	04713	1N5237
2705711	DIODE:HOT CARRIER	28480	1N5711
2710004	DIODE: HOT CARR	07263	FH1100
2710006	DIODE: HOT CARR	28480	5082-2800
2710012	DIODE:VOLT VAR CAP	04713	MV109
2710013	DIODE:LO LKGE-DUAL	32293	DX100
2710014	DIODE,MTCH PR:FH1100	EIP	2710004
2710016	DIODE: HOT CARRIER	28480	5082-2835
2710019	BRDG RECT	14099	SBMB1
2710022	DIODE: PIN	96341	MA47110
2710028	BRDG RECT	04713	MDA990-1
2710029	BRIDE RECT	04713	MDA970-1
2710031	DIODE,GRADED:1N9608-01	EIP	2730960
2710033	DIODE: TUNNEL,SWITCHING	20754	G00010C
2720963	DIODE: 12V ZENER	04713	1N963A
2735235	DIODE: 6.8V ZENER	04713	1N52358
2800004	IC:NUMERIC IND, RED	28480	5082-7730
2800008	LAMP,LED: GREEN	50522	MV5253
2800014	LAMP:LED,YEL DIFFUSED	50522	MV5353
2800015	LAMP:LED,RED	50579	DL-34M
2800016	LAMP:LED,GRN,HI-BRIGHT	0000T	FCV125-BG
3000937	IC:HEX INVERTER	0000X	937N
3007400	IC:QUAD 2INP NAND GATE	0000X	7400N
3007401	IC:QUAD 2INP NAND GATE	0000X	7401N
3007404	IC:HEX INVERTER	0000X	7404N
3007405	IC:HEX INVERTER	0000X	7405N
3007408	IC:QUAD 2INP AND GATE	0000X	7408N
3007411	IC:TRI 3INP AND GATE	0000X	7411N
3007417	IC:HEX BUFFER/DRIVER	0000X	7417N
3007420	IC:DUAL 4INP NAND GATE	0000X	7420N
3007427	IC:TRIPLE 3INP NOR GATE	0000X	7427N
3007432	IC:QUAD 2INP OR GATE	0000X	7432N
3007442	IC:BCD/DEC DECODER	0000X	7442N
3007447	IC:BCD/7SEG DECODER	0000X	7447N
3007454	IC:4WIDE 2INP AOI GATE	0000X	7454N
3007473	IC:DUAL J-K F/F	0000X	7473N
3007475	IC:QUAD LATCH	0000X	7475N
3007476	IC:DUAL J-K F/F	0000X	7476N
3007490	IC:DECADE COUNTER	0000X	7490N
3007493	IC:4BIT BINARY COUNTER	0000X	7493N
3008097	IC:HEX BUFFER	0000X	8097N
3008601	IC:RETRIG ONE SHOT	0000X	8601N
3010616	IC:UHF COUNTER-DIVIDE/4	0000C	SP8616B
3010637	IC:UHF BCD DEC CNTR	0000C	SP8637B
3011039	IC:QUAD TRANSLATOR	0000X	1039P
3011408	IC:8-BIT D/A CONVERTER	0000X	1408L6
3014044	IC:PHASE/FREQ DETECTOR	0000X	4044P
3022206	IC:FUNCTION GENERATOR	0000X	2206CP
3034010	IC:HEX BUFFER/CONVERTER	0000X	4010AE
3034014	IC:P IN/S OUT 8BIT SR	0000X	4014AE
3034511	IC:BCD-7SEG DECODR/DRVR	0000X	4511BE
3035009	IC:P CHAN MOS DIVIDER	0000X	5009N
3037530	IC:MULTIPLYING D/A CONV	0000X	7530JN
3040001	IC:OP AMPL,HI SLEW RATE	06665	OP-01CJ
3040304	IC:VOLT REG	0000X	304
3040305	IC:VOLT REG	0000X	305
3040318	IC:OP AMPL	0000X	318N
3040417	IC:BROAD BAND AMPL	0000X	417
3040555	IC:TIMER,LINEAR	0000X	555V
3040741	IC:OP AMPL	0000X	741CN
3041458	IC:OP AMPL	0000X	1458P1
3041741	IC:OP AMPL,HI SLEW RATE	0000X	1741SCP1
3043049	IC:DUAL/DIFF AMPL	0000X	3049T
3044136	IC:QUAD OP AMPL	0000X	4136PC
3051702	IC:2K UV ERASABLE PROM	34649	1702A
3054040	IC:4-BIT CPU	34649	C4040
3054201	IC:CLOCK GENERATOR	34649	P4201
3070011	IC:S IN/P OUT 8BIT SR	0000X	74LS164P
3070012	IC:4-BIT UP/DN CNTR	0000X	74S168P
3070013	IC:DATA SELECTR/MPXLR	0000X	74LS157P
3070014	IC:DUAL D F/F	0000X	74S74N
3072506	IC:DUAL COMPARATOR	0000X	72506N
3074016	IC:PROGRM MODULO-N CNTR	0000X	4016P
3074123	IC:TTL/MONOSTABLE MV	0000X	74123N
3074153	IC:DUAL 4/1 MULTIPLEXR	0000X	74153N

TABLE 8-3 (Continued). MASTER PARTS LIST

EIP P/N	ITEM DESCRIPTION	MFR	MFR PART NUMBER
3074155	IC:DUAL 2/4LINE DECODR	0000X	74155N
3074157	IC:QUAD 2INP MULTIPLEXR	0000X	74157N
3074176	IC:PRESET DEC COUNTER	0000X	74176N
3074192	IC:DUAL CLOCK W/CLEAR	0000X	74192N
3074196	IC:PST DECADE COUNTER	0000X	74196N
3074393	IC:DUAL 4-BIT BIN CNTR	0000X	74393P
3074490	IC:DUAL DECADE CNTR	0000X	74490P
3090002	IC:QUAD 2INP AND GATE	0000X	74H08N
3110105	IC:TRI OR GATE	0000X	10105L
3110131	IC:DUAL D F/F	0000X	10131L
3110138	IC:BI-QUINARY COUNTER	0000X	10138P
3112000	IC:DIGITAL MIXER/TRANS	0000X	12000P
3112013	IC:TWO-MODULUS PRESCALR	0000X	12013P
3112014	IC:CNTR CONTROL LOGIC	0000X	12014P
3114050	IC:NON-INVERT HEX BUFFR	0000X	14050CP
3150005	IC CUSTOM CHIP - ROM	34649	4308-3251
3510001	INDUCTOR: 0.1UH	72259	DD-0.10
3510003	INDUCTOR: 1.0UH	72259	DD-1.00
3510004	INDUCTOR: 0.22UH	72259	DD-0.22
3510005	INDUCTOR: 2.2UH	72259	DD-2.20
3510007	INDUCTOR: .33UH	99800	1025-08
3510008	INDUCTOR: 0.15UH	99800	1025-00
3510010	INDUCTOR: 1.2UH	99800	1025-22
3510011	INDUCTOR: 0.12UH	72259	DD-0.12
3520007	INDUCTOR: 100 UH	99800	1537-76
3900003	RELAY:SIGNAL.DPDT	11532	712-12
4000XXX	RSTR:COMP 5% TOL. 1/8W	81349	RC05GFXXXJ
4000999	RSTR:COMP-SLECT AT TEST	81349	RC05GFXXXJ
4010XXX	RSTR:COMP 5% TOL. 1/4W	81349	RC07GFXXXJ
4010519	RSTR:COMP 5.1 OHMS 5%	81349	RC07GF5R1J
4010569	RSTR:COMP 5.6 OHMS 5%	81349	RC07GF5R6J
4010999	RSTR:COMP-SLECT AT TEST	81349	RC07GFXXXJ
4020XXX	RSTR:COMP 5% TOL. 1/2W	81349	RC20GFXXXJ
4051002	RSTR:PREC 10K OHM 1%	81349	RN55C1002F
4051332	RSTR:PREC 13.3K OHM 1%	81349	RN55C1332F
4052003	RSTR:PREC 200K OHM 1%	81349	RN55C2003F
4053922	RSTR:PREC 39.9K OHM 1%	81349	RN55C3922F
4054992	RSTR:PREC 49.9K OHM 1%	81349	RN55C4992F
4057151	RSTR:PREC 7.15K OHM 1%	81349	RN55C7151F
4057500	RSTR:PREC 750 OHM 1%	81349	RN55C7500F
4061101	RSTR:PREC 1.1K OHM 1%	81349	RN55D1101F
4061472	RSTR:PREC 14.7K OHM 1%	81349	RN55D1472F
4062152	RSTR:PREC 21.5K OHM 1%	81349	RN55D2152F
4062261	RSTR:PREC 2.26K OHM 1%	81349	RN55D2261F
4062431	RSTR:PREC 2.43K OHM 1%	81349	RN55D2431F
4062871	RSTR:PREC 2.87K OHM 1%	81349	RN55D2871F
4065621	RSTR:PREC 5.62K OHM 1%	81349	RN55D5621F
4065761	RSTR:PREC 5.76K OHM 1%	81349	RN55D5761F
4068661	RSTR:PREC 8.66K OHM 1%	81349	RN55D8661F
4101003	RSTR:PREC 100K OHM .1%	14298	AME55-C3-10038
4102003	RSTR:PREC 200K OHM.25%	14298	AME55-C3-2003C
4104003	RSTR:PREC 400K OHM .5%	14298	AME55-C1-4003D
4108002	RSTR:PREC 80K OHM .1%	14298	AME55-C3-8002B
4110003	RSTR:WW 5 OHM 1% 7W	12436	T7(10PPM)
4110004	RSTR:WW 0.5 OHM 3% 2W	91637	RS-28
4110013	RSTR:WW 0.15 OHM 3% 5W	91637	RS-5
4120004	RSTR:CBN FLM 5.6 OHM 5%	0000L	R25-5.6-5%-1/4W
4120008	RSTR:CBN FLM 8.2 OHM 5%	0000L	R25-8.2-5%-1/4W
4120015	RSTR:CMT FLM 1.24MEG 1%	01121	CC1244F
4120016	RSTR:CMT FLM 2.49MEG 1%	01121	CC2494F
4120017	RSTR:CMT FLM 4.99MEG 1%	01121	CC4994F
4120018	RSTR:CMT FLM 10.0MEG 1%	01121	CC1005F
4130XXX	RSTR:MET OX.100PPM.1/4W	24546	C4/2%/OHMS
4130999	RSTR:MTOX-SLECT AT TEST	24546	C4/2%/XXX
4140030	RSTR:PREC 8K OHM .01%	05591	TYPE 4S8P1S8
4140031	RSTR:PREC 10K OHM .01%	05591	TYPE 4S8P1S8
4140032	RSTR:PREC 20K OHM.025%	05591	TYPE 4S8P1S8
4140033	RSTR:PREC 40K OHM .05%	05591	TYPE 4S8P1S8
4140034	RSTR:PREC 3K OHM .1%	05591	TYPE 4S8P1S8
4140035	RSTR:PREC 6K OHM .1%	05591	TYPE 4S8P1S8
4140039	RSTR:PREC 3.7K OHM .1%	05591	TYPE 4S8P1S8
4150XXX	RSTR:MET OX.100PPM.1/8W	24546	C3/2%/OHMS
4150999	RSTR:MTOX-SLECT AT TEST	24546	C3/2%/XXX
4250001	RSTR:VAR CER 100 OHM	73138	72XWR100
4250003	RSTR:VAR CER 1K OHM	73138	72XWR1K
4250005	RSTR:VAR CER 5K OHM	73138	72XWR5K
4250006	RSTR:VAR CER 10K OHM	73138	72XWR10K
4250008	RSTR:VAR CER 100K OHM	73138	72XWR100K
4250009	RSTR:VAR CER 500 OHM	73138	72XWR500
4250999	RSTR:VAR-SELECT AT TEST	73138	72XWRXXX
4260001	RSTR:VAR CER 10K OHM	80294	3059J-1-103M
4280009	RSTR:VAR WW 500 OHM	73138	89PR-500
4290001	RSTR:VAR 250K/SPDT SW	11236	EF8078/RVF45
4290002	RSTR:VAR 250K/SPDT.WPRF	11236	4P1793RVF-WS321
4500007	SWITCH:P/B.8-STATN (D)	EIP	SRCE CONT DWG
4500008	SWITCH:P/B (PWR IND)	EIP	SRCE CONT DWG
4510001	SWITCH:TOG.SPDT.120V.5A	09353	7101H
4510005	SWITCH:TOG.SPDT.125V 5A	88140	SF21FCW191
4510006	SWITCH:TOG.SPDT.125V10A	88140	SF21SCW191
4520006	SW:SLD.2-DPDT (PWR CHG)	82389	47227LFE
4530008	SWITCH:LEVER (BAND SEL)	76854	555462723-184EA1
4540002	SWITCH.THUMBWHEEL: BCD	23880	900048

TABLE 8-3 (Continued). MASTER PARTS LIST

EIP P/N	ITEM DESCRIPTION	MFR	MFR-PART NUMBER
4703563	XSTR: NPN	07263	2N3563
4704124	XSTR: NPN GP	04713	2N4124
4704126	XSTR: PNP GP	04713	2N4126
4704258	XSTR: PNP RF	07263	2N4258
4704401	XSTR: NPN	04713	2N4401
4704416	XSTR: N-CHAN JFET	04713	2N4416
4704959	XSTR: PNP RF	04713	2N4959
4705983	XSTR: NPN PWR	04713	2N5983
4705989	XSTR: NPN PWR	04713	2N5989
4710002	XSTR: PNP PWR	04713	MJE370
4710003	XSTR: NPN PWR	04713	MJE520
4710007	XSTR: NPN PWR	04713	MJE371
4710009	XSTR: PNP	04713	MJE350
4710010	XSTR: PNP RF	04713	MPS-H81
4710011	XSTR:GRADED 2N5179-RED	EIP	4705179
4710012	XSTR:GRADED 2N5179-YEL	EIP	4705179
4710013	XSTR:GRADED 2N5179-GRN	EIP	4705179
4710014	XSTR:MTCH PR.2N5179-RED	EIP	4710011
4710015	XSTR:MTCH PR.2N5179-YEL	EIP	4710012
4710017	XSTR:NPN RF SW	04713	MMT3960
4710018	XSTR: PNP AMPL	04713	MPS-L51
4710019	XSTR: PNP AMPL	04713	MPS-D55
4710022	XSTR: N-CHAN JFET	01295	TIS73
4710023	XSTR: PNP RF	01295	AST4261
4710025	XSTR: NPN RF	04713	MMT2857
4710026	XSTR: NPN RF	00005	NE73432B
4720002	XSTR: NPN RF	04713	2N3866
4900002	TRANSFORMER,POWER	EIP	SRCE.CONT.DWG.
4900004	TRANSFORMER,POWER	EIP	SPEC.CONT.DWG
5000012	FAN,AXIAL,115VAC	23936	8500
5000052	FUSE HOLDER	75915	348877
5000055	TILT BAIL	21793	453458
5000056	KNOB:RND W/INSERT .51D	86797	RB67-0ML.25SHFT
5000060	KEY,POLARIZING,PCB CONN	04618	530030-1
5000079	FUSE: .750A,SB,3AG,250V	71400	MDL-3/4A
5000101	FUSE: 1.5A,SB,3AG,250V	71400	MDX-1-1/2
5000118	KNOB:LEVER SWITCH	76854	3-4464-201
5210023	COVER,ENCL: TOP	21793	453453
5210024	COVER,ENCL: BOTTOM	21793	453454
5220002	PAD,RUBBER:ENCL FOOT	EIP	M/F:5660004
5230002	GUIDE, PCB	EIP	SRCE CONT DWG
5440002	LINE CORD SET, 3-COND	70903	17250

TABLE 8-3 (Continued). MASTER PARTS LIST

ASSY A1 COMPONENTS (BASIC COUNTER)

REF	EIP P/N
B1 (FAN)	5000012
F1 (115V)	5000101
F1 (230V)	5000079
J1 (PWR RECPT)	2640005
J2 (OPT 09)	2640004
J3 (OPT 01,06,07)	2640004
J4 (10 MHz)	2610024
J111-112	2610024
J113 (P/O A206)	
SMPL RT KNOB	5000056
TILT BAIL	5000055
TOP COVER	5210023
BTM COVER	5210024
MTG FOOT	5220002
AC PWR CORD	5440002
S1 (POWER)	4500008
S102 (115/230)	4520006
S103 (INT/EXT)	4510001
T1 (PWR XFMR)	4900004
XF1 (FUSE HLDR)	5000052

PCB ASSY A101 COUNT CHAIN 1 P/N: 2020036

REF	SAME	EIP P/N
C1		2150003
C2		2300015
C3-4	C1	
C5		2250011
C6-10	C1	
C11-12	C5	
J1		2630009
R1-6		4010332
R7		4010391
R8-11		4010122
R12		4010222
R13-14	R8	
R15-21		4010101
R22	R7	
U1		3007490
U2		3007493
U3		3007402
U4		3007404
U5	U1	
U6	U4	
U7	U3	
U8	U4	
U9	U1	
U10		3007401
U11		3007411
U12	U3	
U13		3007408
U14	U3	
U15		3074176
U16	U4	
U17		3007454
U18		3007400
U19	U3	
U20	U18	
U21		3007405
U22		3007447
U23-24		3007476

PCB ASSY A102 COUNT CHAIN 2 P/N: 2020034

REF	SAME	EIP P/N
C1		2300015
C2-4		2150003
J1-5		2630009
R1		4010222
R2		4010122
R3	R1	
R4-17		4010101
R18-19	R2	
R20		4010569
R21-23	R2	
U1-2		3007447
U3		3007405
U4		3074176
U5		3007475
U6		3074153
U7	U4	
U8	U5	
U9	U6	
U10	U4	
U11	U5	
U12	U4	
U13	U5	
U14	U6	
U15	U4	
U16	U5	
U17	U6	
U18	U4	
U19	U5	
U20		3007432
U21	U5	

PCB ASSY A103 COUNT CHAIN 3 P/N: 2020051

REF	SAME	EIP P/N
C1		2150003
C2		2150999
C3	C1	
C4		2300015
C5-6	C1	
C7		2300010
C8	C1	
C9	C4	
C10	C1	
CR1-8		2705711
CR9		2704154
J1-2		2630009
Q1-3		4710012
Q4		4704124
Q5		4704126
Q6	Q1	
Q7	Q5	
Q8		4710003
R1		4010131
R2		4010361
R3		4010200
R4		4010221
R5		4010121
R6		4010431
R7		4010301
R8		4010102
R9		4010222
R10-12	R8	
R13	R9	
R14	R8	
R15		4010330
R16		4010332
R17	R8	
R18		4010471
R19		4010391
R20		4250009
R21		4010821
R22	R8	
U1		3007405
U2		3074196
U3-5		3074176
U6		3007442
U7-10		3007475
U11		3007427
U12		3007454
U13-14		3074153

PCB ASSY A104 CONTROL 2 P/N: 2020010

REF	SAME	EIP P/N
C1		2150003
C2-3		2300015
C4	C1	
C5		2300010
C6		2150001
C7		2300017
C8-9	C5	
C10-11	C1	
C12-14	C6	
C15	C1	
C16	C6	
CR1-5		2704154
Q1-3		4704126
Q4		4704124
Q5	Q1	
Q6-7	Q4	
Q8-9	Q1	
Q10-15	Q4	
Q16-18	Q1	
Q19	Q4	
R1-3		4010222
R4-6		4010151
R7-9		4010102
R10	R1	
R11		4010681
R12	R1	
R13	R7	
R14	R4	
R15	R1	
R16		4010473
R17	R1	
R18		4010272
R19-20	R1	
R21	R18	
R22		4010103
R23	R18	
R24		4010104
R25-26	R1	
R27		4010101
R28		4010562
R29	R27	
R30	R22	
R31		4010561
R32-33	R7	
R34	R28	
R35	R7	
R36	R11	
R37	R1	
R38	R28	
R39	R22	
R40	R28	
R41	R22	
R42-43	R28	
R44	R22	
R45	R28	
R46	R22	
R47-48	R28	
R49-51	R7	
R52	R11	
R53	R22	
R54	R31	
R55	R7	
R56		4010332
R57-58	R1	
R59-60	R7	
R61-62	R22	
R63	R28	
R64	R1	
R65		4010182

U1		3007404
U2		3007405
U3		3007408
U4	U1	
U5		3007432
U6		3008601
U7		3007400
U8	U6	
U9	U2	

PCB ASSY A105
CONTROL 1
P/N: 2020009

REF	SAME	EIP P/N
C1-2		2150003
C3		2300010
C4-6	C1	
C7		2250001
C8-11	C1	
C12	C7	
C13		2300015
C14	C7	
C15	C1	
C16	C7	
C17-18	C1	
C19	C3	
C20	C1	
C21	C3	
C22	C1	
C23	C13	
C24	C1	
C25	C3	
J1		2630009
Q1		4704258
Q2/4		4710014
Q3	Q1	
Q4	Q2	
Q5		4704126
Q6-7		4704124
R1		4010153
R2		4010221
R3		4010680
R4		4010561
R5		4010101
R6		4010271
R7		4010331
R8		4010151
R9-11		4010471
R12	R7	
R13	R5	
R14	R7	
R15		4010821
R16		4010122
R17		4010182
R18-19		4010102
R20		4010332
R21	R15	
R22	R16	
R23	R20	
R24-25		4010391
R26		4010103
R27	R4	
R28	R24	
R29	R20	
R30-31	R18	
R32		4010222
R33	R20	
R34	R24	
R35	R15	
R36	R16	
R37	R18	
R38	R20	
R39	R18	
R40	R20	
R41-42	R18	
R43	R20	
R44	R15	
R45	R16	
R46	R20	
R47-49	R32	
R50	R26	
R51-52	R32	
R53	R15	
R54	R20	
R55	R18	
R56-57	R32	
R58		4010472
U1		3008601
U2		3007490
U3		3007402
U4		3110105
U5		3090002
U6		3007404
U7	U2	
U8		3011039
U9	U2	
U10		3110131
U11	U6	
U12		3074155
U13		3007432
U14		3007400
U15-16	U2	
U17	U5	
U18	U1	
U19		3035009
U20	U6	
U21	U3	
U22		3007476

PCB ASSY A106
HIGH FREQUENCY
P/N: 2020106

REF	SAME	EIP P/N
C1		2150001
C2-3		2150003
C4		2300015
C5		2300005
C6-7	C2	
C8-9	C5	
C10-11	C2	
C12		2300020
C13		2300024
C14-15	C2	
C16-17	C4	
C18		2260001
C19-20	C2	
C21		2250001
C22	C2	
C23		2250002
C24		2300010
C25-26	C2	
C27	C1	
C28-29	C2	
C30	C1	
C31-36	C2	
C37	C4	
C38	C2	
C39	C24	
C40-41	C2	
C42	C4	
C43	C2	
C44	C24	
CR1		2705231
CR2-5		2704154
CR6		2705230
CR7		2735235
CR8-11	CR2	
CR12-15		2710016
CR16-17	CR2	
CR18	CR12	
CR19		2710033
CR20-21	CR2	
CR22		2705234
CR23	CR12	
CR24-26	CR2	
CR27	CR6	
CR28		2710004
CR29	CR2	
J1-2		2610018
J3		2630009
J4	J1	
J5	J3	
Q1		4710025
Q2-3		4710023
Q4		4710026
Q5		4710022
Q6		4704126
Q7	Q5	
Q8-10		4704124
Q11		4710011
Q12		4704959
Q13-14		4710017
Q15		4710010
Q16		4710013
R1		4130201
R2		4130271
R3		4130510
R4		4130151
R5-6		4130680
R7		4010473
R8-9		4130910
R10-11		4130391
R12		4130102
R13		4130621
R14	R12	
R15	R13	
R16		4130202
R17		4130241
R18		4130472
R19		4010104
R20		4010471
R21		4130561
R22		4130681
R23	R19	
R24-25		4010103
R26		4130473
R27		4130272
R28		4010821
R29		4010511
R30		4010101
R31		4010102
R32		4010510
R33	R12	
R34		4010392
R35		4130120
R36		4010221
R37	R35	
R38		4010202
R39		4010331
R40	R31	
R41	R12	
R42	R31	
R43		4010302
R44		4010272
R45	R32	
R46	R43	
R47	R44	
R48	R29	
R49	R32	
R50	R20	
R51	R43	
R52		4010569
R53	R44	
R54	R20	
R55		4130821
R56	R5	
R57	R52	
R58		4130430
R59	R30	
R60	R27	
R61		4130301
R62	R30	
R63		4010431
R64	R52	

TABLE 8-4. REPLACEABLE PARTS LIST

R65-66		4130560
R67	R52	
R68		4130999
R69		4130390
R70		4130470
R71	R29	
R72	R69	
R73	R52	
R74		4010100
R75		4130750
R76	R21	
R77	R68	
R78	R63	
R79		4010151
R80-82	R24	
R83		4010681
R84-85	R24	
U1		3112013
U2		3070014
U3-5		3074016
U6		3070012
U7		3112014
U8-9		3070011
U10		3070013
U11		3014044
U12		3041458
U13		3040318
U14		3037530
U15		3074490
U16-17		3043049
U18		3010637

PCB ASSY A107
POWER SUPPLY
P/N: 2020077

REF	SAME	EIP P/N
C1		2200010
C2		2300010
C3		2250017
C4	C2	
C5		2200011
C6	C2	
C7		2250009
C8		2300025
C9	C2	
C10		2300008
C11		2150001
C12	C1	
C13	C2	
C14	C10	
C15	C11	
C16	C2	
C17		2200012
CR1-4		2704001
CR5		2710028
CR6		2710029
CR7-8	CR1	
CR9		2720963
CR10-11	CR1	
CR12	CR9	
J1		2620006
Q1		4710002
Q2		4705983
Q3	Q1	
Q4		4705989
Q5		4704126
Q6	Q1	
Q7	Q2	
Q8	Q5	
Q9	Q1	
Q10	Q2	
R1		4010680
R2		4130240
R3		4130821
R4		4110012
R5	R3	
R6		4061472
R7		4250009
R8		4062261
R9		4020430
R10	R1	
R11		4130200
R12		4130101
R13		4110013
R14		4065621
R15	R7	
R16		4062871
R17		4130123
R18	R4	
R19		4130911
R20		4065761
R21		4250003
R22		4062431
R23	R1	
R24		4010101
R25		4010102
R26		4130512
R27		4110004
R28	R19	
R29		4010911
R30	R22	
R31	R7	
R32	R22	
R33	R1	
R34	R24	
R35	R25	
U1-2		3040305
U3-4		3040304

PCB ASSY A108
REF. OSC. BUFFER
P/N: 2020012

REF	SAME	EIP P/N
C1-21		2150003
CR1-5		2704154
J1		2630009
J2		2620029
J3		2620012
J4		2620030
Q1-4		4703563
Q5		4704258
Q6		4710011
Q7-8	Q1	
Q9	Q5	
Q10	Q1	
Q11	Q5	
Q12-13	Q1	
Q14	Q5	
Q15	Q1	
Q16	Q6	
Q17-18	Q1	
Q19	Q5	
R1		4010822
R2		4010392
R3		4010391
R4		4010681
R5		4010202
R6	R1	
R7		4010222
R8		4010751
R9	R5	
R10	R1	
R11		4010181
R12		4010270
R13		4010301
R14		4010100
R15	R1	
R16		4010432
R17	R4	
R18		4010561
R19	R14	
R20		4010112
R21-22		4010519
R23		4130103
R24		4130202
R25		4130621
R26		4130999
R27		4130431
R28	R7	
R29		4010512
R30	R1	
R31		4010362
R32		4010621
R33		4010361
R34		4010431
R35		4130911
R36	R7	
R37	R14	
R38	R1	
R39	R16	
R40	R4	
R41	R18	
R42	R14	
R43	R20	
R44-45	R21	
R46		4010999
U1		3007401

PCB ASSY A109
PRESCALER
P/N: 2020019

REF	SAME	EIP P/N
C1		2100005
C2-5		2100002
C6-7		2250007
C8-10	C2	
C11		2300015
C12	C2	
C13-16		2150003
C17	C2	
C18-21	C13	
C22-23	C11	
C24-25	C13	
C26-27		2300010
CR1-4		2710016
J1		2610018
L1		3510008
P1		2040012
Q1		4710002
Q2		4704124
Q3		4710003
Q4		4710010
Q5/7		4710015
Q6	Q2	
Q7	Q5	
Q8	Q2	
Q9-12		4704126
R1		4010221
R2		4010240
R3	R1	
R4		4010391
R5-6		4000151
R7		4000510
R8		4010184
R9-10		4150390
R11		4010100
R12		4010102
R13		4010681
R14	R8	
R15-16		4051002
R17		4010472
R18		4010332
R19		4010224
R20		4010562
R21-22		4010152
R23		4010122
R24		4000999
R25-26		4000220
R27	R12	
R28		4010999
R29		4010101
R30	R12	
R31-32	R13	
R33		4010103

R34		4010222
R35	R1	
R36		4010331
R37	R12	
R38-39	R21	
R40	R33	
R41		4250003
R42	R18	
R43	R12	
R44	R33	
R45	R20	
R46		4010243
R47	R33	
R48		4010999
U1		3040417
U2		3010616
U3-4		3040741

PCB ASSY A110
DISPLAY
P/N: 2020004

REF	SAME	EIP P/N
DS1-11		2800004
DS12		2800008
DS13-15		2800014
J1-2		2040001
P1		2040013
Q1-7		4710019
R1		4010471
R2		4010122
R3	R1	
R4	R2	
R5	R1	
R6	R2	
R7	R1	
R8	R2	
R9		4010331
R10	R2	
R11		4010681
R12	R2	
R13	R11	
R14	R9	
R15	R2	

PCB ASSY A111
PREAMPLIFIER
P/N: 2020046

REF	SAME	EIP P/N
C1		2250018
C2		2150003
C3		2250012
C4		2300017
C5		2300010
C6	C2	
C7		2300022
C8-9		2300015
C10-11	C2	
C12		2160013
CR1		2735235
CR2-5		2704154
CR6-9		2710016
CR10	CR2	
CR11		2710031
FL1-3		2350017
J1		2620027
J2		2610018
K1		3900003
L1-3	(P/O PCB)	
Q1		4704126
Q2		4704416
Q3		4710012
Q4		4710010
R1		4010510
R2		4020510
R3		4000105
R4		4010911
R5		4010821
R6		4010105
R7		4010512
R8		4010682
R9		4010100
R10		4010472
R11		4010470
R12		4010181
R13		4010121
R14	R5	
R15		4010182
R16	R5	
R17		4130102
R18		4130999
R19		4010221
R20		4130999
R21		4010331
R22-23		4010102
R24	R17	
R25		4130910
R26		4010569
R27		4130101
R28-29	R22	
R30		4010511
U1		3043049

PCB ASSY A113
CNTR INTERCONNECT
P/N: 2020069

REF	SAME	EIP P/N
C1		2250011
C2		2300015
CR1-3		2704154
CR4-5		2710004
CR6		2710016
J1	(NOT USED)	
J2		2620014
J3		2620044
J4		2620047
J5		2620016
J6	J4	
J7-8		2630009
J9-10	J4	
J11	J7	
Q1		4704124
R1/S9		4290001
R2	(NOT USED)	
R3		4010151
R4-5		4010432
R6		4010750
R7-8		4010222
R9		4010472
R10		4010182
R11		4010331
R12-13	R10	
R14	R6	
R15		4010332
R16	R10	
R17-29		4010242
S1-8		4500007

ASSY A116
TCXO
P/N: 2030002

(NO REPLACEABLE COMPONENTS)

PCB ASSY A122
MICROPROCESSOR
P/N: 2020107

REF	SAME	EIP P/N
C1		2300025
C2		2300008
C3-4		2250008
C5-6		2150003
C7		2150006
C8-9	C5	
C10		2350024
C11-12		2250003
C13		2300021
C14	C5	
C15		2300005
C16	C2	
C17	C5	
C18		2150010
C19		2250018
C20	C5	
C21		2250006
C22		2250026
C23	C5	
C24	C1	
C25-29	C5	
CR1-16		2704154
J1		2630010
J2-5		2630009
Q1		4704124
Q2		4710019
Q3-7	Q1	
Q8		4710022
Q9	Q1	
Q10		4704126
R1		4130102
R2		4130201
R3		4130101
R4		4010339
R5		4010244
R6		4010103
R7		4010473
R8		4010104
R9		4010101
R10		4010271
R11	R6	
R12		4010202
R13-14		4130999
R15-18		4130103
R19		4130203
R20		4130301
R21		4130472
R22		4130242
R23		4130123
R24	R12	
R25-27	R19	
R28-29		4010273
R30		4130183
R31		4130182

TABLE 8-4. REPLACEABLE PARTS LIST

R32	R8	
R33		4010105
R34		4010183
R35-36		4130513
R37	R13	
R38	R6	
R39		4010999
R40	R19	
R41		4130273
R42		4130302
R43	R19	
R44-45		4130152
R46	R19	
R47-50		4130820
R51		4010510
U1		3054201
U2		3054040
U3		3150005
U4		3034010
U5-6		3070011
U7		3022206
U8		3044136
U9		3041458
U10		3037530
U11-12		3034014
Y1		2030013

PCB ASSY A123
AUXILIARY DISPLAY
P/N: 2020108

REF	SAME	EIP P/N
C1-2		2300024
CR1		2710016
DS1-2		2800018
DS3-4		2800015
DS5-8	DS1	
J1		2630010
Q1-3		4704126
R1		4010360
R2-8		4010271
R9-10		4010104
R11		4010241
R12	R2	
U1		3034511
U2-3		3070011
U4		3007417
KEYBOARD		2020109

ASSY A2 COMPONENTS
(CONVERTER TRAY)

REF	EIP P/N
A2Q1	4710009

PCB ASSY A201
SOURCE/AMPLIFIER (P/O
MODULE ASSY 2010091)

REF	SAME	EIP P/N
C1-2		2150003
C3		2300008
C4		2300015
C5-10	C1	
C11		2160016
C12		2160007
C13-15	C1	
C16		2350003
C17		2160013
C18		2160006
C19	C1	
C20		2250005
C21	C1	
C22		2160005
C23		2350001
C24		2160008
C25		2160004
C26-28	C1	
C29-30	C22	
C31	C11	
C32	C1	
C33-34		2150001
C35	C16	
C36	C17	
C37	C18	
C38	C1	
C39		2250002
C40		2350002
C41-42		2160010
C43-44	C1	
C45	C40	
C46	C41	
C47-49	C1	
C50	C39	
C51	C1	
C52	C40	
C53	C41	
C54-55	C1	
C56		2350022
C57-58	C39	
C59-61	C1	
C62		2300010
C63		2150999
C64-66	C1	
C67		2250014
C68	(NOT USED)	
C69-80	C1	
CR1		2710006
CR2		2704154
CR3		2710012
CR4	CR2	
CR5	CR1	
CR6-11	CR2	
FL1-4		2350017
J1-3		2610010
L1-2	(NOT USED)	
L3		3520007
L4		3510003
L5-6	(P/O PCB)	
L7	L4	
L8-9	(P/O PCB)	
L10		3510010
L11		3510001
L12	L4	
L13	(P/O PCB)	
L14-15	L10	
L16	L4	
L17	(P/O PCB)	
L18-21	L10	
L22		3510011
L23	L4	
L24-33	L10	
P1		2040112
Q1-2		4704124
Q3		4710012
Q4		4710010
Q5	Q3	
Q6-7		4704416
Q8	Q3	
Q9	Q4	
Q10		4704126
Q11		4710013
Q12	Q6	
Q13-14	Q3	
Q15-16		4720002
Q17		4710003
Q18-21	Q10	
Q22	Q1	
R1		4010202
R2		4010510
R3		4130682
R4		4130392
R5		4130271
R6		4130202
R7	R4	
R8	R3	
R9-11		4010511
R12		4010391
R13		4010111
R14		4130241
R15		4130182
R16		4130122
R17-18		4130622
R19		4130562
R20		4130912
R21		4130302
R22	R16	
R23		4130821
R24		4130102
R25		4010102
R26		4010472
R27		4130511
R28		4130221
R29	R27	
R30	R15	
R31	R28	
R32		4130332
R33		4130243
R34		4010243
R35	R33	
R36	R24	
R37		4130113
R38		4010393
R39		4130201
R40	R24	
R41	R20	
R42	R21	
R43	R16	
R44	R23	
R45	R24	
R46	R4	
R47	R21	
R48	R39	
R49		4130300
R50		4130999
R51	R17	
R52	R24	
R53	R33	
R54	(NOT USED)	
R55		4010561
R56	R2	
R57-58	R17	
R59	R24	
R60		4130223
R61	R24	
R62		4130103
R63	R37	
R64	R23	
R65		4130272
R66		4010272
R67		4130472
R68		4130391
R69	R32	
R70		4010101
R71		4010103
R72-78	R70	
R79		4130471
R80-81		4130222
U1		3112000
U2		3110138
U3		3014044
U4-5		3040741

PCB ASSY A202
CONV CONTROL 2
P/N: 2020116

REF	SAME	EIP P/N
C1		2150008
C2-5		2150003
C6		2300020
C7	C2	
C8		2150001
C9		2300008
C10	C2	
C11	C8	
C12		2300010
C13	C2	
C14	C12	
C15-16	C2	
C17		2300015
C18-21	C2	
C22		2250003
C23	C2	
C24		2250025
C25		2250999
C26-27	C2	
CR1		2700827
CR2		2704154
CR3		2704757
CR4		2704001
CR5		2705225
J1-2		2630009
J3		2620031
Q1-8		4704401
Q9		4704126
Q10		4704124
Q11		4710018
Q12	Q9	
R1-7		4010512
R8		4010826
R9		4010396
R10		4010206
R11		4120018
R12		4120017
R13		4120016
R14		4120015
R15		4052003
R16		4250006
R17		4010272
R18		4104003
R19		4010103
R20-21		4010564
R22	R17	
R23		4102003
R24	R19	
R25	R17	
R26		4101003
R27	R19	
R28	R17	
R29		4108002
R30	R19	
R31	R17	
R32		4140033
R33		4010123
R34	R17	
R35		4140032
R36		4010203
R37	R17	
R38		4140031
R39	R17	
R40		4140030
R41		4057500
R42-43		4140035
R44		4130183
R45		4130113
R46		4120999
R47		4140034
R48		4054992
R49		4250003
R50		4053922
R51		4010152
R52		4140039
R53		4280009
R54		4110003
R55	R47	
R56		4010162
R57		4010391
R58-59		4010102
R60	R57	
R61	R19	
R62	R33	
R63		4010332
R64	R17	
R65		4010624
R66	R36	
R67	R17	
R68		4130472
R69		4010999
R70		4130912
R71		4130123
R72	R58	
R73		4010392
R74	R33	
R75		4130822
R76	R19	
R77		4010101
U1		3074393
U2-3		3041458
U4		3007400
U5-6		3007404
U7-9		3074176
U10		3040555
U11		3051702
U12		3114050
U13		3007408
U14		3011408
U15		3040741

PCB ASSY A203
CONV CONTROL 1
P/N: 2020066

REF	SAME	EIP P/N
C1		2150001
C2		2160010
C3-9	C1	
C10-11		2150003
C12	C1	
C13		2150005
C14		2250018
C15	C10	
C16		2350024
C17		2250021
C18	C10	
C19		2300008
C20	C10	
C21		2300021
C22		2300023
C23	C10	
C24-28	C1	
C29-30		2250006
C31		2160007
C32		2160005
C33-34	C1	
C35-36	C10	
C37		2250026
C38		2150009
C39		2300003
C40	C19	
C41		2250025
C42	C19	
C43-44	C10	
C45		2300010
C46	C10	
C47	C22	
C48-49	C10	
C50	C22	
C51-52	C10	
C53	C45	
C54-56	C10	
CR1		2704154
CR2/3		2710014
CR4	CR1	
CR5		2710013
CR6		2705231
CR7		2705227
CR8		2705237
CR9	CR1	
CR10/11	CR2/3	
L1		3510003
L2	(P/O PCB)	
L3		3510001
L4-5	(P/O PCB)	
L6		3510004
L7-8	(P/O PCB)	
P1	(P/O PCB)	
P2		2040010
P3		2040011
P4	P2	
Q1		4710012
Q2		4710010
Q3		4710017
Q4	Q1	
Q5		4704124
Q6	Q1	
R1		4010151
R2		4010272
R3		4010101
R4		4010511
R5		4010270
R6		4010222
R7		4010330
R8		4010102
R9	R7	
R10		4010221
R11		4010271
R12	R8	
R13		4010331
R14		4010750
R15		4010184
R16-17		4130103
R18	R15	
R19	R14	
R20		4010332
R21		4010622
R22		4250006
R23	R8	
R24		4010113
R25	R11	
R26		4010363
R27		4010472
R28		4010103
R29	R8	
R30		4010301
R31-32		4010201
R33		4010182
R34	R27	
R35		4010683
R36	R28	
R37		4010152
R38	R8	
R39		4010123
R40		4010202
R41	R28	
R42	R27	
R43	R24	
R44-45	R28	
R46	R4	
R47		4010820
R48	R31	
R49	R5	
R50	R8	
R51-52	R6	
R53		4010510
R54		4010131
R55	R53	
R56	R13	
R57	R8	
R58	R6	
R59		4010751
R60-61		4010111
R62	R13	
R63	R53	
R64		4250001
R65-66	R15	

TABLE 8-4. REPLACEABLE PARTS LIST

R67		4010912
R68		4010822
R69	R21	
R70		4010303
R71	R8	
R72-73	R28	
R74-75		4057151
R76	R39	
R77		4010133
R78	R3	
U1		3041741
U2		3072506
U3		3040741
U4		3043130
U5	U2	
U6		3074123
U7		3007473
U8		3007400
U9		3007408
U10-11	U7	
U12		3007405
U13		3043049
U14	U6	
U15		3011408
U16		3074393
U17		3007420
U18	U6	

ASSY A204/A205/A206
AUTOMATIC INPUT
LEVEL CONTROL (ASSY'S
PART OF MATCHED SET)
P/N: 2010061

PCB ASSY A204
VIDEO AMPL (PART OF
MODULE ASSY 2010045)

REF	SAME	EIP P/N
C1		2250018
C2		2150003
C3		2160002
C4	C2	
C5		2250006
C6-9	C2	
C10	C5	
C11-14	C2	
C15	C5	
C16-19	C2	
C20-21		2250009
C22	C2	
C23		2150001
C24-25	C2	
C26	(NOT USED)	
C27	C23	
C28-30	C2	
C31	C5	
C32-35	C2	
C36	C5	
C37-40	C2	
C41	C5	
C42-45	C2	
C46	C5	
C47	C2	
C48	C2	
C49		2300010
C50		2160002
C51		2160015
C52-55	C2	
C56	C5	
C57-64	C2	
C65		2250027
C66		2250002
C67	C2	
C68	C49	
C69	C2	
C70	C66	
CR1-2		2710022
CR3-4		2710004
CR5	(NOT USED)	
CR6	CR3	
CR7		2704370
CR8		2704001
CR9		2704154
FL1	(NOT USED)	
FL2-4		2350017
J1		2610017
J2-5		2610010
L1		3510005
L2	(JUMPER)	
L3-9	(P/O PCB)	
L10		3510007
L11-20	(P/O PCB)	
Q1		4700026
Q2-3		4710011
Q4-5		4710012
Q6-7	Q1	
Q8	Q4	
Q9		4710013
Q10-11		4704124
Q12-13		4704126
Q14	Q10	
Q15	Q12	
Q16	Q1	
Q17	Q4	
R1		4130132
R2		4130201
R3		4130421
R4		4130242
R5		4130560
R6		4120008
R7		4130911
R8		4010222
R9		4130999
R10		4130621
R11	R4	
R12	R5	
R13	R6	
R14	R7	
R15	R9	
R16	R10	
R17	R4	
R18	R5	
R19		4130100
R20	R7	
R21		4010511
R22	R9	
R23	R10	
R24		4130510
R25	R10	
R26		4010112
R27		4130121
R28		4010221
R29		4120004
R30	R27	
R31	R4	
R32	R29	
R33	R7	
R34	R6	
R35	R9	
R36	R10	
R37	R4	
R38	R5	
R39	R6	
R40	R7	
R41		4010102
R42	R9	
R43	R10	
R44	R4	
R45	R5	
R46	R7	
R47	R19	
R48	R9	
R49	R10	
R50	R4	
R51	R5	
R52		4130821
R53		4010999
R54	R19	
R55	R24	
R56		4130471
R57		4010121
R58	R24	
R59		4130152
R60		4130272
R61		4250008
R62		4130133
R63		4130103
R64		4130391
R65-66	R41	
R67		4010473
R68	R61	
R69-70		4010822
R71		4010103
R72-73		4010163
R74	R41	
R75		4130122
R76	R63	
R77		4130910
R78		4130163
R79	R1	
R80		4130222
R81-82	R63	
R83		4130102
R84	R52	
R85		4250003
R86		4130681
R87	R71	
R88		4068661
R89		4130912
R90		4010471
R91		4130392
R92-95		4010240
R96	R90	
R97		4130123
R98		4130101
R99		4010680
R100	R91	
R101	R67	
R102		4130562
R103		4130752
R104-105	R8	
R106		4130180
R107		4130662
R108		4130303
R109		4010224
R110	R64	
R111	R80	
U1		3040001
U2-4		3040741
U5		3041741

ASSY A205
MIXER
PART OF P/N: 2010061

(NO REPLACEABLE
COMPONENTS)

ASSY A206
PIN DIODE ATTENUATOR
PART OF P/N: 2010061

(NO REPLACEABLE
COMPONENTS)

ASSY A207
YIG COMB GENERATOR
P/N: 2010097-02

(NO REPLACEABLE
COMPONENTS)

PCB ASSY A208
CONV INTERCONN
P/N: 2020044

REF	SAME	EIP P/N
J1		2620042
J2		2040027
J3		2620014

PROGRAMMING OPTION PC BOARD (NOTE: THIS BOARD IS USED FOR SEVERAL OPTIONS; PARTS USAGE WILL VARY ACCORDINGLY.)

PCB ASSY A115
PROGRAMMING
P/N: 2020104

REF	SAME	EIP P/N
C1		2150003
C2		2300015
C3-4	C1	
J1-6		2630009
P1		2640004
R1		4010151
U1-4		3007405
U5		3007408
U6		3007400
U7-9		3074157

OPTIONS 03, 04, 05:
OVENIZED OSCILLATOR
ASSY A112

REF	EIP P/N
OPT 03	2030001-01
OPT 04	2030001-02
OPT 05	2030001-03
R1 (T/B ADJ)	4260001
W14	2040009

PCB ASSY A114
OVEN OSC PWR SUPPLY
P/N: 2020022

REF	SAME	EIP P/N
C1		2200014
C2		2300010
C3		2250017
C4		2300008
CR1		2710019
CR2-3		2704001
Q1		4710007
R1		4110004
R2		4062152
R3		4250009
R4		4061101
T1		4900002
U1		3040305

OPTION 06: PROGRAMMABLE OFFSETS

PCB ASSY A100
P/N: 2020033

REF	SAME	EIP P/N
C1		2300015
C2-4		2150003
J1		2630009
Q1		4704124
R1-3		4010222
U1		3007402
U2		3007404
U3-4		3007476
U5		3007408
U6-8		3074192

OPTION 09: BCD OUTPUT

PCB ASSY A117
BCD OUTPUT
P/N: 2020039

REF	SAME	EIP P/N
C1-2		2150003
C3		2300015
C4	C1	
CR1		2704154
J1-3		2630009
J4		2620014
P1		2640004
Q1		4704401
R1		4010220
R2-3		4010103
U1-8		3000937

TABLE 8-4. REPLACEABLE PARTS LIST

SECTION 9

CIRCUIT SCHEMATICS & DESCRIPTIONS

COMPONENT LOCATORS

9-1. GENERAL

9-2. Schematics and Component Locators are arranged by Assembly number (A101, A102, etc.). Circuit descriptions and circuit theory are shown on the same or adjacent pages. All assembly related drawings and diagrams have the same figure number, but have different suffix letters (9-6A, 9-6B, etc.).

9-3. Parts Lists and Ordering Information will be found in Section 8.

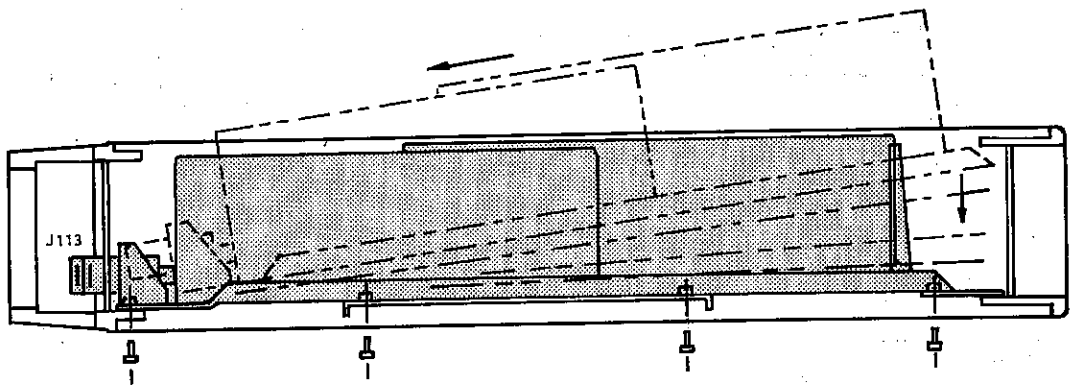
9-4. Unless otherwise specified, the following notes apply to all figures in this section.

a. Resistance values in ohms.

b. Capacitance values in microfarads ("pf" values in picofarads).

c. Connector reference numbers may not appear on part.

d. SAT = Selected at Test. Nominal value shown; part may not be installed. MP = Matched Pair.

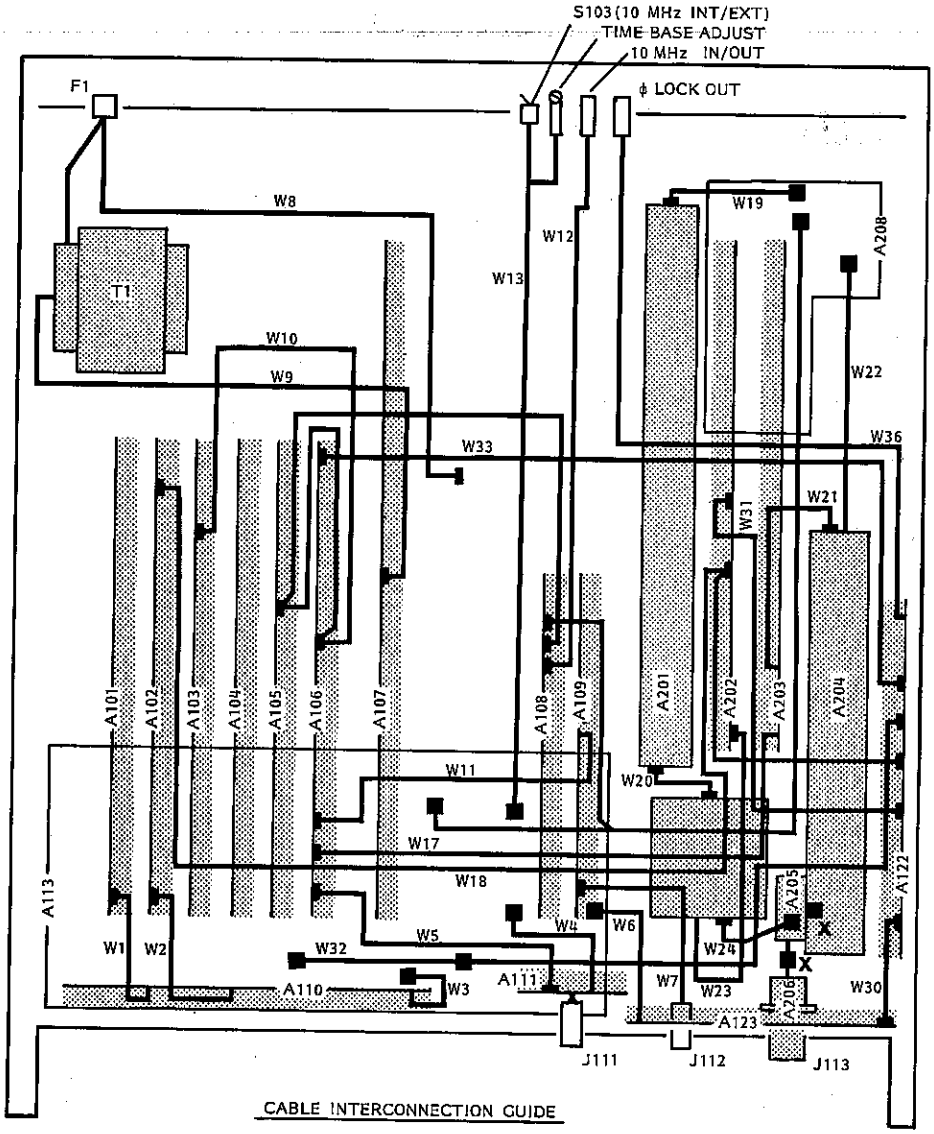


FIELD INSTALLATION OF CONVERTER ASSEMBLY

1. WITH TOP AND BOTTOM COVERS REMOVED FROM BASIC COUNTER, LOWER CONVERTER INTO POSITION AS SHOWN IN DIAGRAM: TILT J113 DOWN AND FORWARD THROUGH HOLE IN FRONT PANEL.
2. INSTALL SIX 6-32 SCREWS FROM BOTTOM SIDE OF COUNTER INTO CAPTIVE NUTS ON CONVERTER. ALIGN J113 CONCENTRICALLY WITH FRONT PANEL HOLE; TIGHTEN SCREWS.
3. PLUG CABLES W16, W17, AND W18 INTO MATING CONNECTORS ON BASIC COUNTER (SEE CABLE INTERCONNECTION GUIDE); REPLACE COVERS. REVERSE ABOVE PROCEDURE TO REMOVE CONVERTER.

FIELD INSTALLATION OF PRESCALER ASSEMBLY

1. WITH TOP COVER REMOVED, PLUG PRESCALER (A109) INTO A113-XA109. MOUNT J112 IN FRONT PANEL HOLE.
2. PLUG CABLES W7 AND W11 INTO MATING CONNECTORS PROVIDED ON MODULES (SEE CABLE INTERCONNECTION GUIDE); REPLACE COVER.



CABLE INTERCONNECTION GUIDE

BASIC COUNTER

FROM	CABLE	TO
A110J1	W1	A101J1
A110J2	W2	A102J1
A110P1	W3	A113J2
A111P1	W4	A113J4
J111	X	A111J1
A111J2	W5	A106J1
A123P1	W6	A113J6
J112	W7	A109J1
REAR PNL	W8	J101
P102 (T1)	W9	A107J1
A108J1	W10	A105J1
A106J3		A103J2
A109P2	W11	A106J2
P104	W12	A108J2
P103	W13	A113J5
A122J1	W30	A123J1
A122J4	W32	A113J7
A113J8		
A122J5	W33	A106J5
A206P2	W34	A204J4
A206P1	W35	A204J3
A122P1	W36	P105 (REAR PNL)

CONVERTER

FROM	CABLE	TO
A208J2	W16	A113J3
		A108J4
A203P3	W17	A106J4
A202J2	W18	A102J4
		A122J3
A201P1	W19	A208J1
A201J1	W20	A207J2
A203P2	W21	A204J2
A204P1	W22	A208J3
A202J3	W23	A207J3
		A2Q1
A205P1	W24	A207J1
A205P2	X	A204J1
A205J1	X	A206P1
A202J1	W31	A122J2

LEGEND:

- X — Direct-coupled (No cable assy)
- Cable - to - Assembly
- Cable - to - Assembly
- Cable - to - Cable

CAUTION: Use care when unplugging ribbon cable connectors. Use removal tool for extraction (EIP P/N: 5000094).

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047A

FIGURE 9-1
ASSEMBLY LOCATOR
CABLE INTERCONNECTIONS

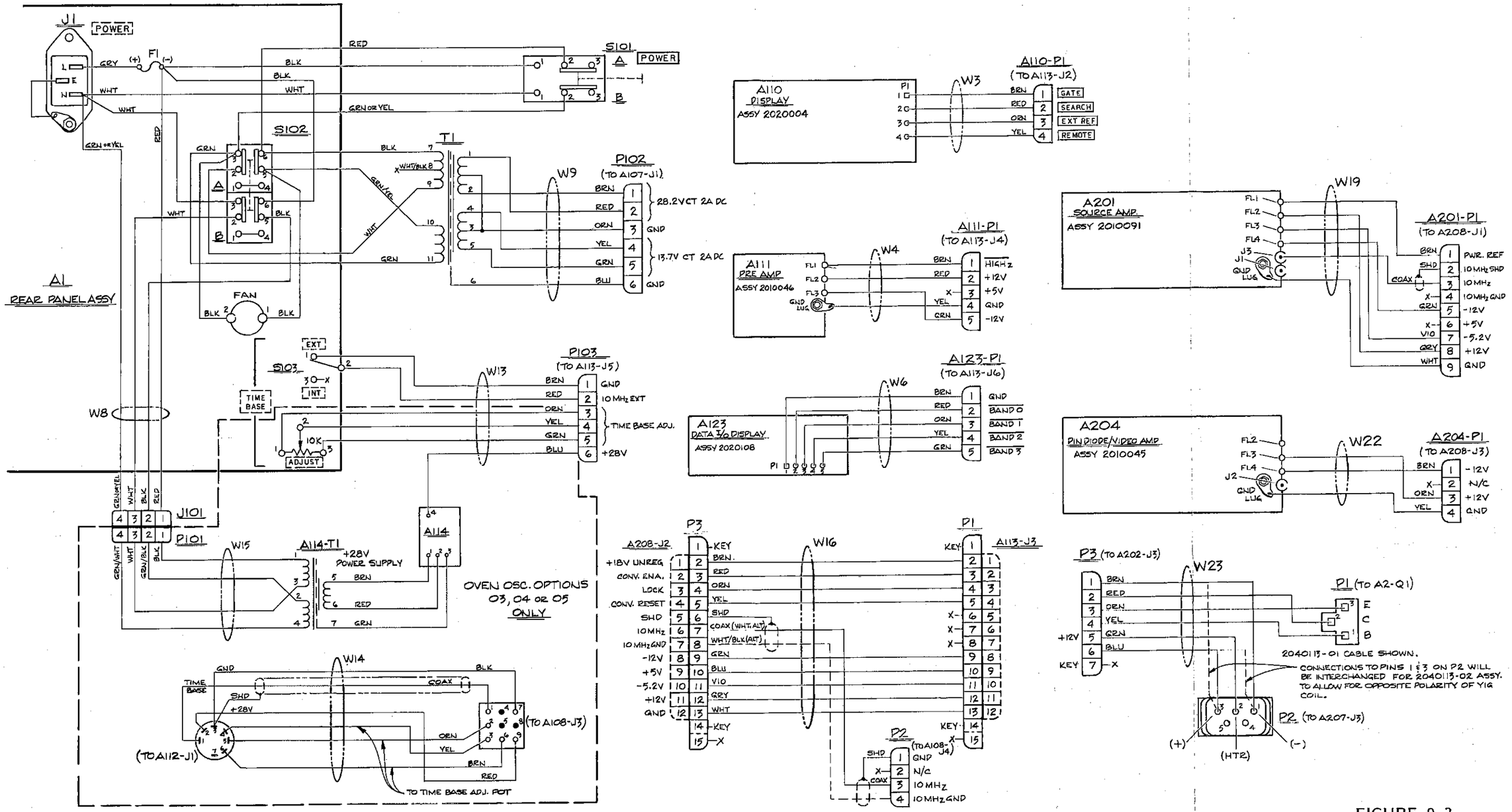
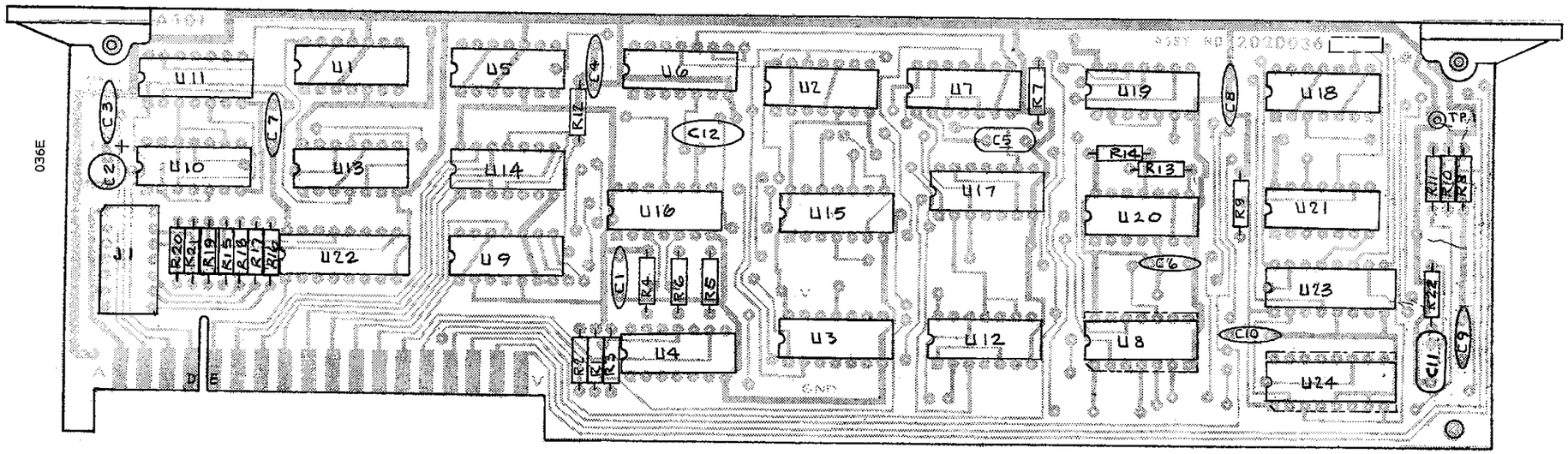


FIGURE 9-2
INTERCONNECTION
DIAGRAM
371 COUNTER

007A



GATE TIME	÷5 COUNT	B	C	D
1 sec.	5	0	0	0
100 ms.	4	0	0	1
10 ms.	3	1	1	0
1 ms.	2	0	1	0
	1	1	0	0
	0	0	0	0

TABLE 9-3B
U15 PRESETS

	LATCH - DISPLAY DIGIT POSITION										
	1	2	3	4	5	6	7	8	9	10	11
GATE TIME	10 GHz	1 GHz	100 MHz	10 MHz	1 MHz	100 kHz	10 kHz	1 kHz	100 Hz	10 Hz	1 Hz
1 sec.	1	2	3	4	5	6	7	8	9	10	11
100 ms.	1	2	3	4	5	6	7	8	10	11	-
10 ms.	1	2	3	4	5	6	7	10	11	-	-
1 ms.	1	2	3	4	5	6	10	11	-	-	-
	NUMBER OF DCU SUPPLYING DATA TO LATCH										

TABLE 9-3A
DISPLAY DIGIT POSITION vs. SUPPLYING DCU

FIGURE 9-3A
COMPONENT LOCATOR
COUNT CHAIN 1 (A101)

COUNT CHAIN 1, 2, AND 3

Count Chain Boards 1, 2, and 3 (A101, A102, and A103) perform most of the actual frequency counting functions of the direct counter. The main components are: (1) a counting chain, (2) a storage unit, and (3) the display multiplexer.

The counting chain consists of a string of ten cascaded decimal counting units (DCUs), preceded by a quinary (÷5) counting unit. The quinary counter is sufficiently fast to follow the output of the binary (÷2) counter in the High Frequency Board, forming the first DCU. The remaining DCUs are each a standard integrated circuit, having four output lines to indicate the state of the counter at any given time.

The storage unit is a string of quad latches, one for each of the eleven DCUs of the counting chain. An enable signal to the storage unit causes it to load the information from the DCUs.

The display multiplexer processes the information held in the eleven elements of the storage unit. The output of the storage unit is converted to the seven line code needed to drive the seven segments of each display digit. Power is applied to each digit sequentially for 25% of the time.

Physical Organization

The Count Chain is divided among three PC Boards: A101, A102, and A103, as follows:

Board A103 contains the first quinary unit, the following four DCUs, quad latches to load the information in the DCUs, and a multiplexer to place the information in proper time sequence for the front panel display. A variable +5 VDC supply for display brightness is also provided.

Board A102 includes the six remaining DCU's of the counting chain, a set of associated quad latches, and two multiplexers. Two decoders convert the multiplexer outputs to the seven line code which drives the visual display.

Board A101 includes the third decoder-driver, buffer circuits for the front panel RESOLUTION switches, timing circuits for the multiplexer and display. A101 also contains circuitry which suppresses zeros to the left of the first significant digit.

COUNT CHAIN 1 (A101)

Count Chain 1 (A101) generates the correct timing sequence and control commands for the multiplex system, provides leading zero blanking of the display, and controls shifting of data from DCU to DCU in the counting chain in response to changes in gate time length.

In addition, A101 accepts the inputs from the front panel RESOLUTION switches, and processes them into control signals for the multiplex system and the Time Base Generator on Control 1 (A105). A101 also contains the third decoder driver for the display.

Multiplex System Operation

The multiplex system is composed of three individual multiplex channels designated MUX 1, MUX 2, and MUX 3. Each MUX channel includes a four-to-seven line decoder-driver which drives directly segments of the front panel display. MUX 1 controls the four most-significant digits of the display (10 GHz, 1 GHz, 100 MHz and 10 MHz). MUX 2 controls the middle three digits and MUX 3 the four least-significant digits. The input information for MUX 1, 2, and 3 is obtained from the eleven quad-latch units on Count Chains 2 and 3 (A102 and A103).

In order for each multiplex circuit and decoder to drive four digits, the multiplex timing sequence is broken down into four intervals designated Time Frames 1 through 4 (TF1 - TF4). Only one display digit in each channel is illuminated in a given Time Frame, as determined by the display digit selectors. The actual number displayed by the selected digit is determined by segment drive from the decoder-driver which drives all corresponding segments in that channel in parallel. If one of the selected digits is not to be illuminated, its segment drive is canceled by a blanking signal to the appropriate decoder-driver. Table 9-3C shows, for each channel and for each of the gate times, the relationship of the Time Frames to MUX address, the DCU addressed, the display digit selected by the MUX, and whether the drive is enabled.

For each available gate time, Table 9-3A shows the resulting position in the display at which the information from each DCU is presented. The DCUs not displayed in shorter gate times are those removed from the counting chain, as described in the paragraphs on Count Chain 3 (A103).

In addition to blanking digits 9, 10, and 11 of the display (as shown in Table 9-3A), three more digits may be blanked by depressing the appropriate RESOLUTION switches. The gate time remains at 1 ms. in these positions.

The MUX timing sequence is actually three groups of four time frames. The first two groups occur at a rate of 2.5 MHz, the last at 25 kHz. The fast groups are used only to gather zero suppression information; display occurs only during the slow group.

Multiplex Sequence Generator

Clock pulses for the multiplexer are obtained from a 2.5 MHz clock signal derived from the 10 MHz Time Base Oscillator (A116 or A112). This signal is processed through a circuit composed of DCUs U1 and U5, ÷16 U2, the inverters of U6, and the gates of U11. The "SET 9" inputs of the DCUs are tied together, so that applying a high level to this input causes the 2.5 MHz clock to be fed through the gates to U2 at a 2.5 MHz rate.

With a low "SET 9" the input to U2 is one-hundredth the 2.5 MHz rate, or 25 kHz. The "SET 9" inputs to U1 and U5 are the inverted D output from U2, which is high when U2 is reset. The clock to U2 is then at a 2.5 MHz rate for eight pulses after reset. The D output then switches, and the clock rate drops to 25 kHz for the next four pulses. The A and B outputs of U2, plus their complements, are combined in the four NOR gates of U7 to produce the four MUX timing signals TF1, TF2, TF3, and TF4. The output TF4 is combined with U2 output D, and applied to the J input of flip-flop U23B. The clock to U23 and U24 is the same as the input to U2. The end of the fourth slow clock pulse then triggers U23B which resets U2. The clock pulses then return to the 2.5 MHz rate. The next pulse resets U23B and returns U1, U2, and U5 to their initial states.

The result is to produce a frame consisting of eight MUX time intervals at the 2.5 MHz rate, followed by four at the 25 kHz rate. One extra clock pulse resets the generator. The drive to the front panel display from U10 is gated off by the D output of U2 during the eight fast pulses in this train.

Count Chain Data Shift Controls

As the length of the Gate Time is varied by changing the front panel RESOLUTION switches, the counting chain on A103 is also modified by removing DCUs from the string. This is described in the Circuit Description of Count Chain 3 (A103). In the 1 Hz RESOLUTION setting (1 sec. Gate Time), all eleven DCUs are in the counting chain. With 10 Hz RESOLUTION (100 ms. Gate Time), the seventh (10 kHz position) DCU is bypassed. With 100 Hz RESOLUTION the seventh and eighth DCUs are bypassed, and with 1 kHz RESOLUTION the seventh through ninth DCUs are bypassed.

As indicated in Table 9-3A, with shorter gate times, the information in the eighth through eleventh DCUs must be shifted into lower numbered latches (7 through 10) to read out and be displayed in the proper front panel position. The data shift controls which accomplish this function are produced in ICs U9, U13, U14, U15, and U16.

To allow the data shift to take place on A103, presettable DCUs are used in the counting chain. The output lines of the eleventh DCU feed the data input lines of the tenth DCU. The tenth DCU feeds data to the ninth DCU, the ninth feeds data to the eight, and the eighth feeds data to the seventh. When a LOAD DATA command is applied to one of these DCUs, it then loads data from and assumes the same state as the higher numbered DCU to its right. To shift data one place left in the highest five DCUs of the counting chain (DCUs 7 through 11), it is necessary to apply the data LOAD pulses in sequence to DCUs 7, 8, 9, 10, and then a reset pulse to DCU 11 (load zero). If the load pulses were applied simultaneously to all DCUs, they

would all go immediately to zero. The necessary sequence of pulses is produced by a 4-10 line decoder on A103 which is driven by a DCU on A101. The DCU is stepped through states 0 to 9 by a clock input, with the 1, 3, 5, 7, and 9 outputs of the decoder activating the load inputs of DCUs 7, 8, 9, 10, and 11 respectively. Every ten inputs to the data shift DCU on A101 cause the data in the DCUs on A103 to shift left one position.

To place the counting chain data in the proper position after the end of each gate time interval, clock pulses must be applied to the data shift DCU. With 1 second gate time, no pulses are required; with 100 ms. gate time, ten pulses are required; with 10 ms. gate time, 20 pulses; and with 1 ms. gate time, 30 pulses. The number of clock pulses is regulated by presettable DCU U15 and associated gates in U13, U14, and U16.

The ÷5 part of U15 is preset during the gate time to the states shown in Table 9-3B. Data inputs to produce them are the four gate control lines. The ÷2 part of U15 directly controls the gate through which the 2.5 MHz clock is applied to data shift DCU U9. With 1 second gate time, the binary is not preset, and no data shift clock pulses occur. With shorter gate time settings, the ÷2 is set during gate time, with data shift clock pulses occuring after gate time is complete. Every ninth pulse to the data shift DCU (U9) produces an output through AND gate U13 which is applied to the ÷5 input of U15. The input to U15 is combined with the D output in another AND gate, and applied to the ÷2 input. When the ÷5 count reaches zero state, the ÷2 state is also zero, and the data shift clock turns off. Depending upon the ÷5 preset state, either 0, 10, 20, or 30 clock pulses have occured, and the counting chain data has shifted 0, 1, 2, or 3 places to the left.

Additional gates inhibit the Sequence Generator during data shift. Update Data is also inhibited during this time.

Display Selector Drive Generator

This drive is actually the same as the MUX Time Frame signals during the slow scan. The signals TF1 - TF4 provide one input to each of the four NAND gates of U10. The other four inputs are tied together with the D output of U2. This D output is high only after the first eight fast scan signals (first two groups of TF1 - TF4) have occurred, and the slow scan (third group of TF1-TF4) is taking place. The NAND gate outputs are the inputs to the digit selector drivers on Display Board (A110).

Signal Generators for Blanking and Gate Time Controls

These generators operate on the inputs from the six front panel RESOLUTION switches. They are processed in the inverters of U4 and U8, and the NOR gates of U3 and U12, to produce nine output control signals. Five of these are used on A101 principally to control display blanking. The remaining four are used externally, as well as on A101. The four lines, one of which is high for each gate time, are fed to the gate generator on A105, which then determines the gate time. The signals are also fed to Count Chain 3 (A103) where they control the length of the counting chain as the gate time is changed. One of these four signals, plus the remaining five, are used on A101 to control least significant digit blanking by the RESOLUTION switches. Three outputs of U20 produce blanking signals in Display Driver 2, by combining MUX timing outputs TF2, TF3, and TF4 with the RESOLUTION switch signals from U4 and U8. This produces blanking in readout digit 7 (as indicated in Table 9-3C), plus blanking of digits 5 and 6 in resolution settings for 100 kHz and 1 MHz. U17 produces the blanking signals in Display Drive 3 (as indicated in Table 9-3C), plus complete blanking (TF1 - TF4) in the 100 kHz and 1 MHz resolution settings.

Leading Zero Suppression Circuitry

The portion of A101 related to leading zero suppression is detailed in Figure 9-3C. This function is accomplished in two steps. Initially, the circuit determines if any of the three channels contains non-zero data. If all data is zero, it disables the blanking and displays all zeros. If there is non-zero data, it locates the first channel containing this data.

The most vital portion of the zero suppression circuitry is contained within the decoder-drivers themselves. This is a zero detection circuit which is enabled by the ripple blanking input (RBI). If RBI is enabled (low), the presence of zero data causes the ripple blanking output (RBO) to be energized (low). The decoder-driver also contains a blanking input (BI) which blanks the digit when energized (low). BI and RBO are internally tied together so that the pin designated BI/RBO serves both as an input and an output. Thus, if RBI is enabled, zero data will energize RBO, which is equivalent to energizing BI, and the digit is blanked. Thus, a digit may be blanked either by applying a low-level to BI/RBO, or by the presence of zero data when RBI is enabled.

The first circuit function is to determine if any of the three channels contain non-zero data. All flip-flops are reset enabling the RBI on all decoder-drivers. As the multiplex system rapidly scans through its first four Time Frames, any non-zero data in a decoder-driver will be indicated by the RBO going high. This in turn enables the J input of the corresponding flip-flop. The next timing pulse sets that flip-flop and disables the RBI of that decoder-driver. At the end of the first multiplex group, the presence of any non-zero data is indicated by a set flip-flop. A set flip-flop enables the J input of the following flip-flop. This insures that non-zero data in any decoder-driver causes all flip-flops further down the chain to be set within two additional Time Frames.

If all data is zero, then the gating is such as to allow the eight clock pulse (TF4 of the second fast group) to set the first two flip-flops and enable the third. The ninth clock pulse then sets the third flip-flop. This then disables all ripple blanking inputs so no blanking will occur with all zero data.

The remaining task is to determine the first channel with non-zero data. Gates are arranged so that the ninth clock pulse will reset the first flip-flop which is in the "set" state via the K input, and thus enable the corresponding RBI, prior to the start of the slow scan. The internal ripple blanking circuitry will then blank all zeros until the first non-zero data is present.

Gate Time	Sequence Time Frame in MUX Sequence	MUX Address a	MUX Address b	CHANNEL 1 DCU Addressed	CHANNEL 1 Display Digit Selected	CHANNEL 1 Drive Enable	CHANNEL 2 DCU Addressed	CHANNEL 2 Display Digit Selected	CHANNEL 2 Drive Enable	CHANNEL 3 DCU Addressed	CHANNEL 3 Display Digit Selected	CHANNEL 3 Drive Enable
1 sec.	TF-1	0	0	1	1	+	5	5	+	8	8	+
	TF-2	1	0	2	2	+	6	6	+	9	9	+
	TF-3	0	1	3	3	+	7	7	+	10	10	+
	TF-4	1	1	4	4	+	11	7	–	11	11	+
100 ms.	TF-1	0	0	1	1	+	5	5	+	9	8	+
	TF-2	1	0	2	2	+	6	6	+	10	9	+
	TF-3	0	1	3	3	+	7	7	–	11	10	+
	TF-4	1	1	4	4	+	8	7	+	8	11	–
10 ms.	TF-1	0	0	1	1	+	5	5	+	10	8	+
	TF-2	1	0	2	2	+	6	6	+	11	9	+
	TF-3	0	1	3	3	+	7	7	–	8	10	–
	TF-4	1	1	4	4	+	9	7	+	9	11	–
1 ms.	TF-1	0	0	1	1	+	5	5	+	11	8	+
	TF-2	1	0	2	2	+	6	6	+	8	9	–
	TF-3	0	1	3	3	+	7	7	–	9	10	–
	TF-4	1	1	4	4	+	10	7	+	10	11	–

TABLE 9-3C
GATE TIME vs. SEQUENCE TIME FRAME and DCU ADDRESSED

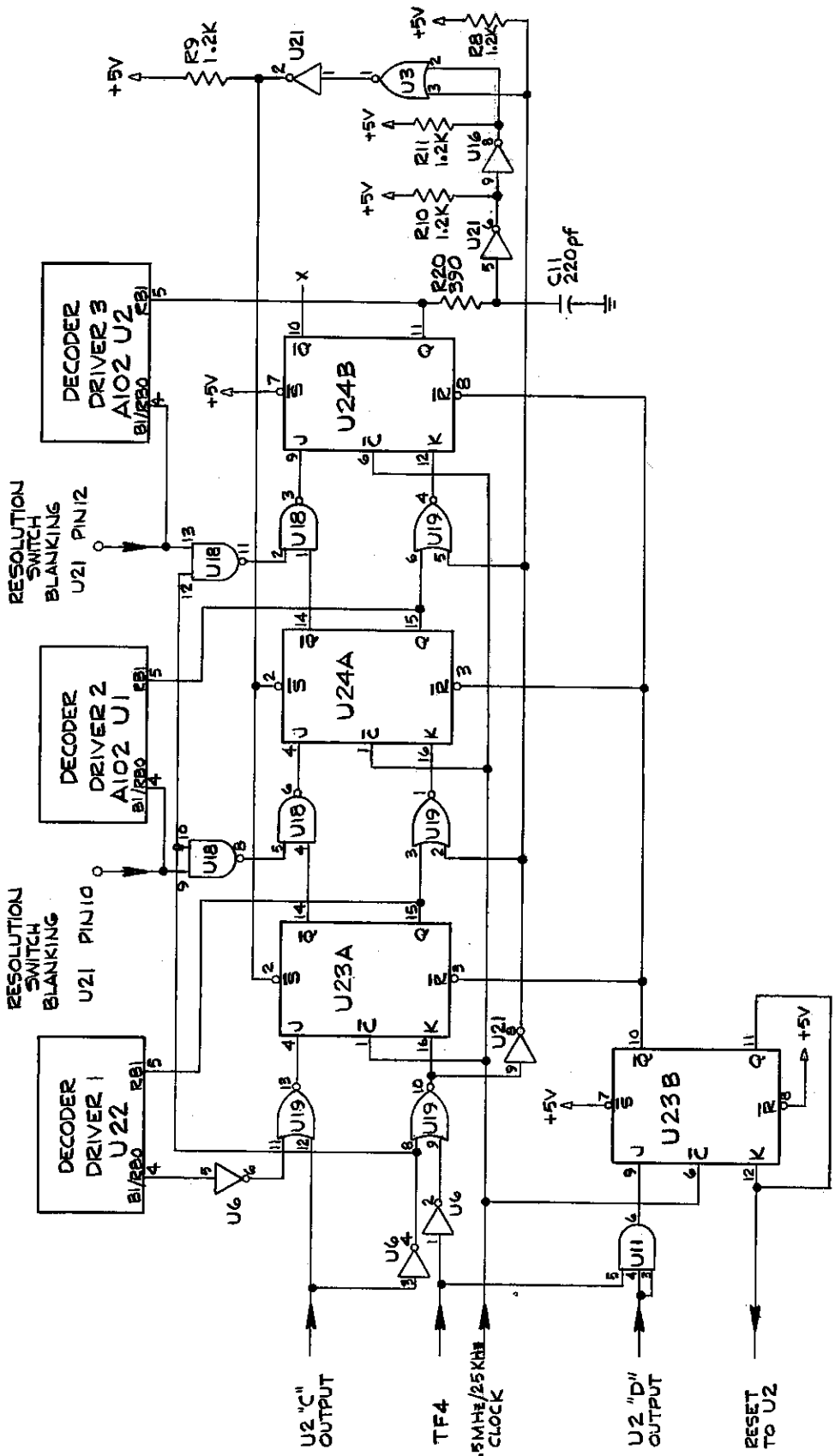
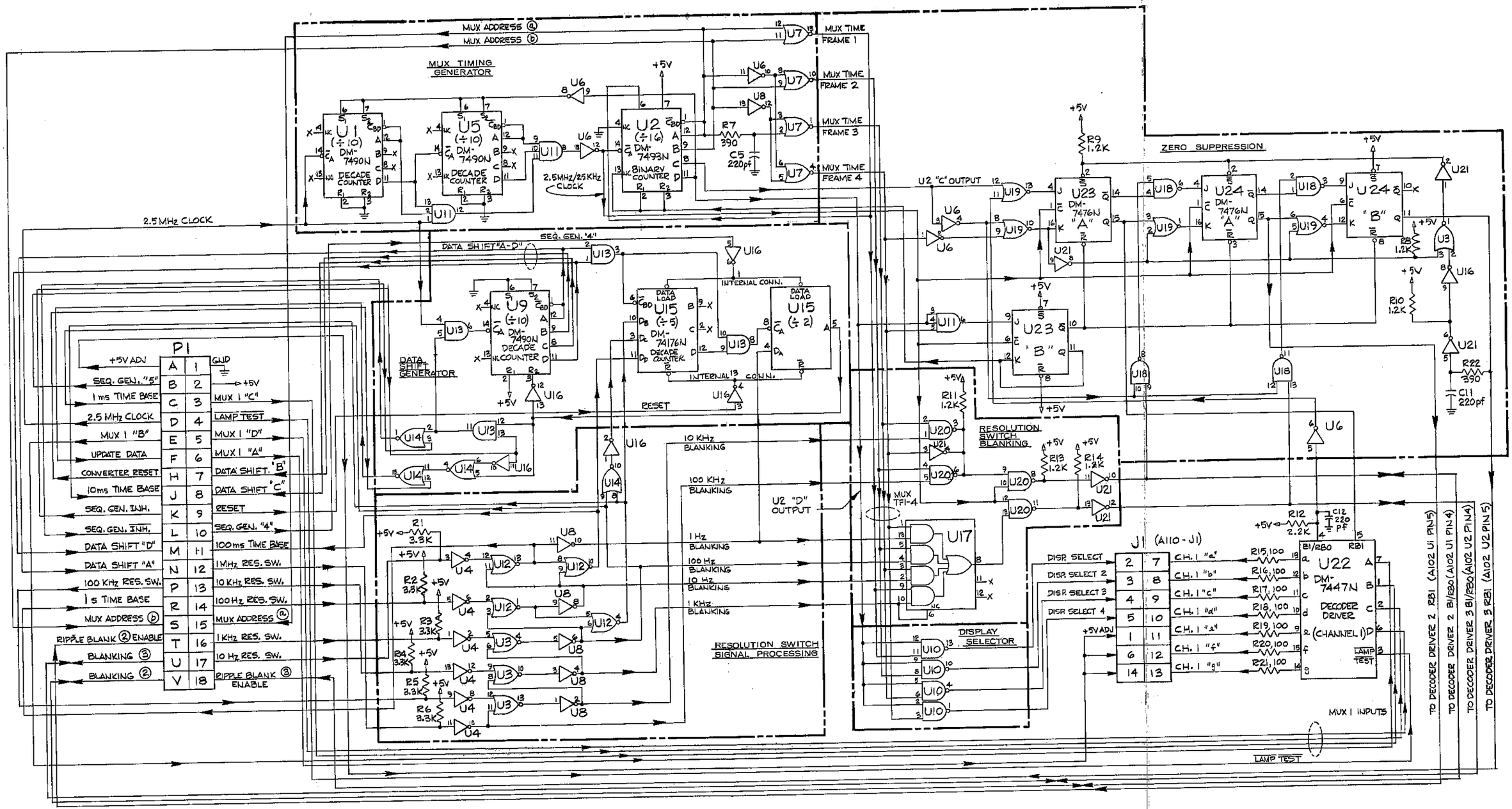
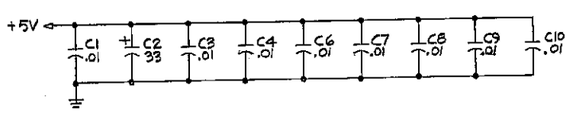


FIGURE 9-3C
PARTIAL SCHEMATIC
LEADING ZERO SUPPRESSION

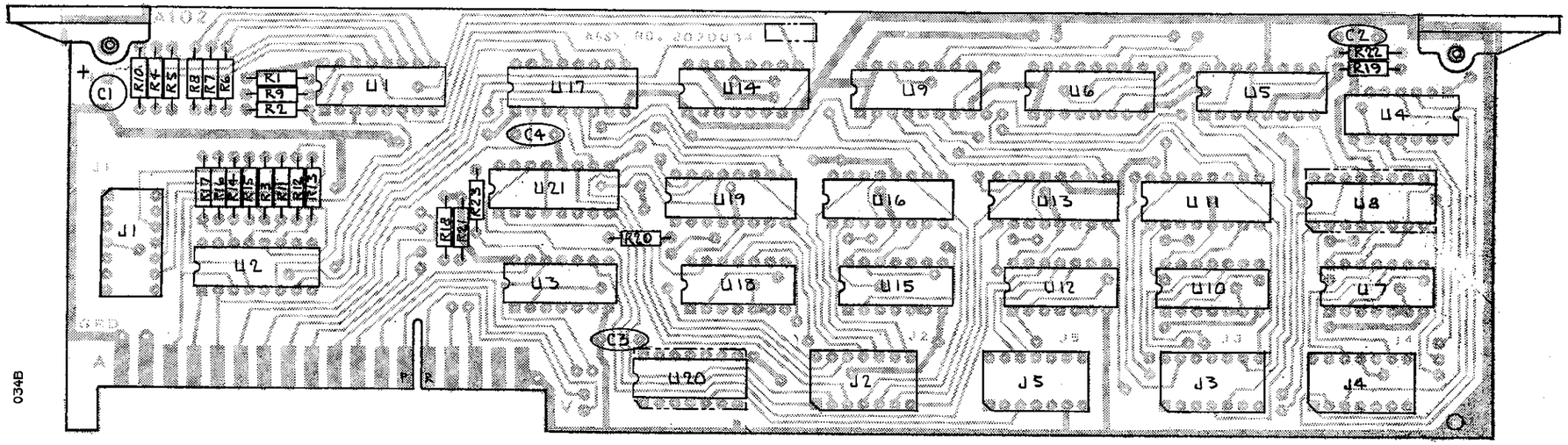




I.C. NO.	TYPE	PIN NO. GND	PIN NO. +5V
U1, U5, U9	DM7490N	10	5
U2	DM7493N	10	5
U3, U7, U12, U14, U19	DM7402N	7	14
U4, U6, U8, U16	DM7404N	7	14
U10	DM7401N	7	14
U11	DM7411N	7	14
U13	DM7408N	7	14
U15	DM74176N	7	14
U17	DM7454N	7	14
U18, U20	DM7400N	7	14
U21	DM7405N	7	14
U22	DM7447N	8	16
U23, U24	DM7476N	13	5

FIGURE 9-3B
SCHEMATIC DIAGRAM
COUNT CHAIN 1 (A101)

036C



0348

COUNT CHAIN 2 (A102)

A102 is similar to A103, being simply a continuation of the counting chain that begins on A103. Six DCUs on A102 (U4, U7, U10, U12, U15, and U18) combine with the five DCUs on A103 for a total of eleven in the counter. Each of these six are presettable. They are programmed by data lines either from the Converter (when it is being used), or from external inputs when IF Offset Option 06 is used.

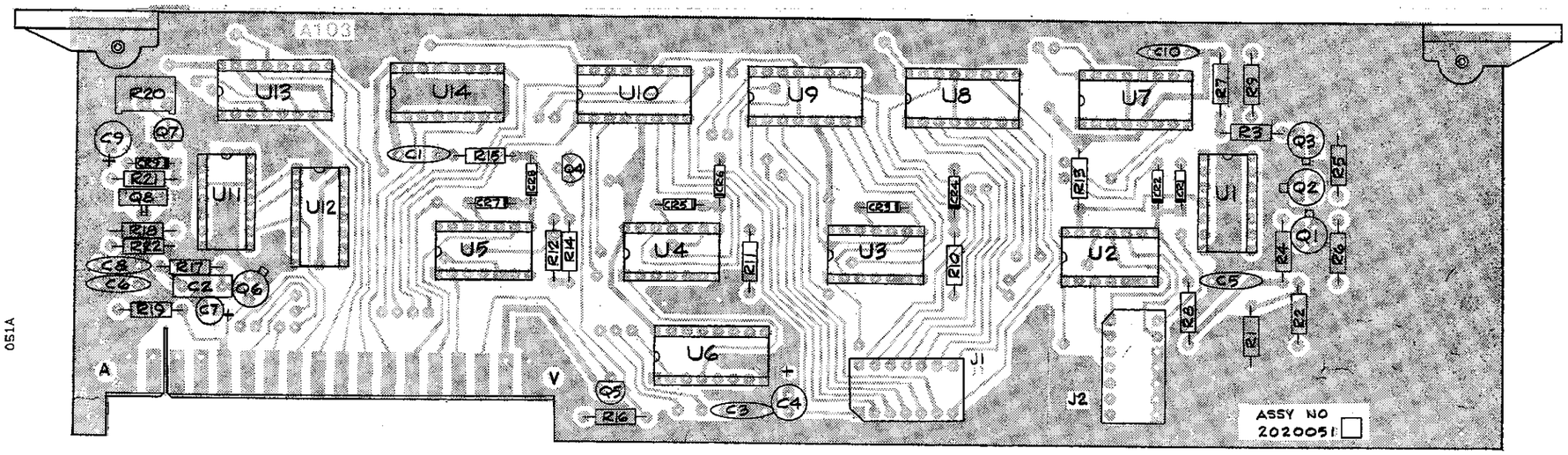
Each of the six DCUs has an associated quad-latch (U5, U8, U11, U13, U16, and U19) to store the DCU information. An additional latch (U21) stores the information from the last DCU on A103 (U1), which does not have a quad-latch on that board. Two sets of multiplexers (U6 and U9, and U14 and U17) transfer the information from the latches to the display drivers. Two decoder-drivers (U1 and U2) convert the four line BCD information from the two multiplexers into the seven-line code necessary to drive the segments of the front panel display. Separate inputs to these decoders allow the display to be blanked, or to display all eights in the Visual Display Test. (A more detailed description will be found in the paragraphs titled "Leading Zero Suppression Circuity".)

FIGURE 9-4A
COMPONENT LOCATOR
COUNT CHAIN 2 (A102)

IC NO.	PIN NO.	
	+5V	GND
U1, U2, U6, U9 U14, U17	16	8
U3, U4, U7, U10, U12, U15, U18, U20	14	7
U5, U8, U11, U13, U16, U19, U20	5	12

FIGURE 9-4B
SCHEMATIC DIAGRAM
COUNT CHAIN 2 (A102)

034A



COUNT CHAIN 3 (A103)

A103 receives BCD and carry signals from the High Frequency Board (A106). The carry signal is processed thru one to four decade dividers (U2-U5), with the carry output at P1 pin E sent to the Count Chain 2 Board (A102). Gate width commands from the RESOLUTION switches, control data routing and shifting to place the data in proper position for display. Display data for 1 Hz thru 1 kHz information is stored on this board, with mux commands from the Count Chain 1 Board (A101) controlling the transfer of this data to the front panel display.

Data from the first DCU on A106 enters at J2. The data consists of four TTL logic bits giving the BCD information from the first decade, and a 60% duty cycle ECL logic signal which is the carry output from the first decade.

The ECL carry signal enters the ECL-to-TTL converter on the base of Q1. R1 and R2 provide a 95 ohm termination to -1.4 V (open circuit voltage at J2 pin 3). R5 and R6 provide a reference voltage of -1.5 V at the base of Q2. Q1, Q2, and Q3, form a differential cascode amplifier operating in the over-driven mode as a level translator. R3 prevents the TTL output signal from going negative.

The TTL carry signal enters a cascade of four DCU's (U2-U5). The carry output from A103 can be selected from any one of the four DCU's by a 4-wide, 2-input AND-OR-INVERT gate (U12). The selection of the carry output is determined by the RESOLUTION switches. For 1 second gate times, the output comes from U5; for a 0.1 sec gate time, from U4, etc.

There are four latches on A103 (U7-U10) which contain the information to be displayed by the 1 Hz thru 1 kHz digits. The input to these latches comes from the first four decade dividers: input to U7 comes from the decade divider on the High Frequency Board (A106), input to U8 from A103U2, to U9 from A103U3, and to U10 from A103U4.

When the counter is operated in shorter gate time than one second, the decade dividers contain correspondingly higher digit information. For example: For a 0.1 second gate, the first DCU (on A106) contains the 10 Hz information; for a .01 second gate, 100 Hz information, and for a 1 ms gate, 1 kHz information. In order for this information to be displayed properly, BCD information in the DCU's is shifted to the right before it is transferred to the storage latches. The data shift occurs in sequence from right to left; that is, the data moves from U4 to U5, then from U3 to U4, from U2 to U3, and finally from J2 to U2. This shift sequence is controlled by the four command signals: Data Shift A thru Data Shift D, generated on A101. This series occurs once for 10 Hz resolution (100 ms gate), twice for 100 Hz resolution (10 ms gate), and three times for 1 kHz resolution and above (1 ms gate). During the data shift process, the normal clock inputs to the DCU's must be inhibited. This is accomplished by one third of U11, and the four diode gates (CR1, CR4, CR6, and CR8). These gates are held off during sequence 5 when the data is being shifted.

Reset of the four DCU's is controlled by the counter reset line, and occurs after the data is read into the latches and before the next counter gate period. The inverted BCD information from the latches goes to J1 for use with the BCD Output option.

The non-inverted BCD data from the four latches goes to a 4-by-4 mux consisting of U13 and U14. This data is then sent four bits at a time, to the Count Chain 2 Board (A102), where it is converted into 7-segment display information to drive the front panel LED display. The control signals for the mux switch come from A101 and are comprised of two signals: mux address a, and mux address b. These two signals form a binary code to give four addresses: 0, 1, 2, and 3, as shown in Table 9-5A.

SELECTED INPUT	ADDRESS	
	A	B
0	0	0
1	1	0
2	0	1
3	1	1

TABLE 9-5A
MULTIPLEX ADDRESS

FIGURE 9-5A
COMPONENT LOCATOR
COUNT CHAIN 3 (A103)

PERIOD	FUNCTION	DURATION	LOCATION
9	COUNTER RESET	10 µs	-
0	3 MSD $\overline{\text{SET}}$	10 µs	U12 pin 9
1	OFFSET ENABLE	10 µs	U12 pin 10
2	GATE GENERATOR SET	10 µs	U12 pin 11
3	GATE GENERATOR ENABLE	10 µs	U12 pin 12
4	GATE PERIOD	GATE + 10 µs	U12 pin 7
5	$\overline{\text{DATA UPDATE}}$	10 µs	U3 pin 10
6/7	PRINT	20 µs	U14 pin 6
8	DISPLAY PERIOD	Variable	U9 pin 11

TABLE 9-7A

SEQUENCE GENERATOR COMMANDS

Commands are generated as shown in Table 9-7A. (Period numbering is determined by the output state of U9.) The sequence proceeds as follows:

Period 9: The starting point in the cycle. All counting chain DCU's are reset.

Period 0: In Band III, the YIG/Comb Generator frequency is preset.

Period 1: Used to preset counter in conjunction with Offset Option 06.

Period 2: The Gate Generator is set.

Period 3: The Latch Binary (U10B) is reset, enabling the Gate Binary (U10A). The 10 MHz clock (U8 pin 7) is applied to the Gate Generator.

Period 4: The Gate Generator is enabled and inhibits the Sequence Generator (U13 pin 8) for the duration of the gate time. The incoming signal to the counter is counted during this period.

Period 5: The accumulated data in the counting chain DCU's is loaded into the latches.

Period 6/7: The PRINT command is generated indicating the presence of data on units equipped with Digital Output Option 09.

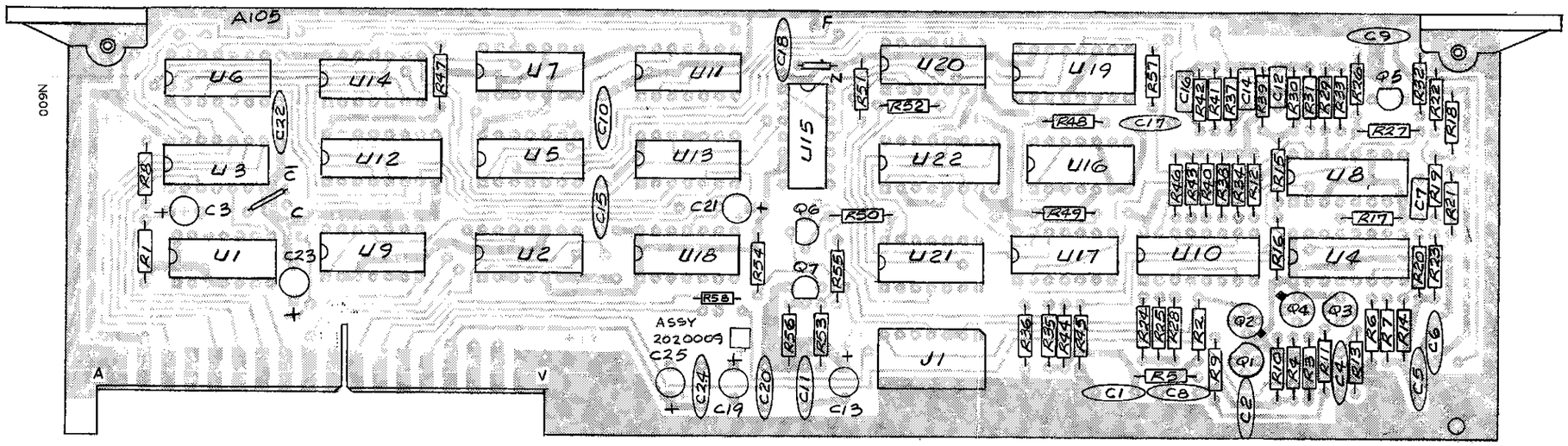
Period 8: The Display Period. The Display Generator is turned on and inhibits the Sequence Generator during this time. The duration of the period is determined by the front panel SAMPLE RATE control.

TABLE I			
I.C. NO	TYPE	PIN NO.	
		GND	+5V
1, 4	DM7404N	7	14
2, 9	DM7405N	7	14
3	DM7408N	7	14
5	DM7432N	7	14
6, 8	DM8601N	7	14
7	DM7400N	7	14

ALL DIODES ARE P/N: 2704154.

FIGURE 9-6B
SCHEMATIC DIAGRAM
CONTROL 2 (A104)

010F



CONTROL 1 (A105)

This unit contains the circuitry to generate the counter control sequence and the gate time interval. These functions are derived from the 10 MHz Time Base Oscillator.

Clock Generator

Transistors Q1 through Q4 form a Schmitt Trigger to convert the 10 MHz time base signal to a square wave suitable to drive the ECL gates of U4. These outputs are further gated and translated to TTL levels in U8.

Sequence Generator

This circuit produces the main control cycle of the counter by generating a sequence of commands. It consists primarily of an address generator U9, and a decoder U12.

Clocking is performed at a 100 kHz rate by dividing the 10 MHz TTL clock in DCU's U2 and U7. An output of 2.5 MHz is also obtained at U7 pin 12 for the multiplexer clock on Count Chain 1 (A101). The gates of U5 are arranged so that both the 100 kHz and the 2.5 MHz signals are trains of 50 ns wide pulses.

The 100 kHz pulse train drives address generator U9, which produces a four line BCD code. The A and B outputs of U9 address U12, while the C output selects which of the two decoders is active. This generates sequential control signals, one on each of eight lines. Two more signals are obtained using the D output of U9 by itself, or combined with the A output. The gate inputs to U12 (pins 2 and 14) are turned off during switching and when not required, by an OR gate in U13. This eliminates any outputs due to switching transients.

Several internal counter operations inhibit the sequence generator. In addition, Digital Output Option 09, and Remote Programming Option 07, allow the sequence to be externally inhibited.

Gate Generator

The Gate Generator provides the correct gate time interval as required by the front panel RESOLUTION switch settings. The time interval is controlled by selecting an integral number of cycles of the 10 MHz Time Base Oscillator. This then turns the Gate Binary U10 on and off appropriately.

The major element of the Gate Generator is a programmable multi-decade divider, U19. By applying the proper address as shown in Table 9-7B, division ratios from 10^3 to 10^6 can be obtained. A 1 MHz input is then used to generate intervals from 1 ms to 1 second. DCU U16 divides the 10 MHz clock signal to provide the 1 MHz input for U19. The address is obtained by processing the four gate control signals from A101.

For operation in Band II, it is necessary to expand the gate time by a factor of four, since the incoming frequency is divided by four. This is accomplished by disabling Q5. The 2.5 MHz signal from U2 and U7 then appears at U8 pin 15 during the gate time and is combined with the 10 MHz signal to produce a 2.5 MHz pulse train at U17 pin 3. If Q5 is enabled, then the 10 MHz pulse train will appear there.

The Q_B output of U22 is combined in U17 with the 10 MHz clock and the A and D outputs of U16 to produce the Time Base Gate Level at U17 pin 6. This arrangement guarantees that the gate time interval is precisely determined by the 10 MHz signal itself.

It is necessary that the Q_B output be no more than one microsecond duration. The two flip-flops of U22 are interconnected in such a manner as to produce a single one microsecond pulse every time the output of U19 goes low.

Display Time Generator

This generator consists of U18, U15, Q6, Q7 and associated circuitry. Triggering the multivibrator U18 generates a pulse whose width is determined by C21 and the resistance of the front panel SAMPLE RATE potentiometer. Q6 is a current amplifier to increase the available range, while DCU U15 is used to scale the range by a factor of ten. The result is a display time period variable from approximately 60 ms to 40 seconds. U18 is triggered by the SEQUENCE GENERATOR "8" appearing at pin 2. Once turned on, feedback from Q7 to pin 4 holds the unit in its free running state until pin 3 goes low. Pin 3 input is derived from the output of DCU U15. The Display Time Generator output (U3 pin 12) is then used as one of the Sequence Generator Inhibit inputs.

The Display Time cycle begins with SEQUENCE GENERATOR "9" setting U15 (pin 7) to the "9" state which inhibits U18 (pin 3) from triggering. When SEQUENCE GENERATOR "7" begins, U15 is reset (pin 3), thus enabling U18. Period "8" triggers U18 (pin 2) and the Sequence Generator is then held in period "8" until U15 counts to 9, at which time the display period ends.

Application of the front panel HOLD command at U13 pin 8, holds U15 in the reset position so that the Sequence Generator is permanently inhibited in period 8.

To assist troubleshooting of the Sequence Generator, a Cycle Speed jumper is provided. If this jumper is moved from +5 (Normal) to ground (Fast), the R(1) input (U15 pin 2) is brought low, and the Display Generator is inhibited, thus reducing the display time to 10 microseconds.

CONTROL LINE			DIVISION RATIO
2^0	2^1	2^2	
1	1	0	10^3
0	0	1	10^4
1	0	1	10^5
0	1	1	10^6

TABLE 9-7B
PROGRAMMABLE DIVIDER

FIGURE 9-7A
COMPONENT LOCATOR
CONTROL 1 (A105)

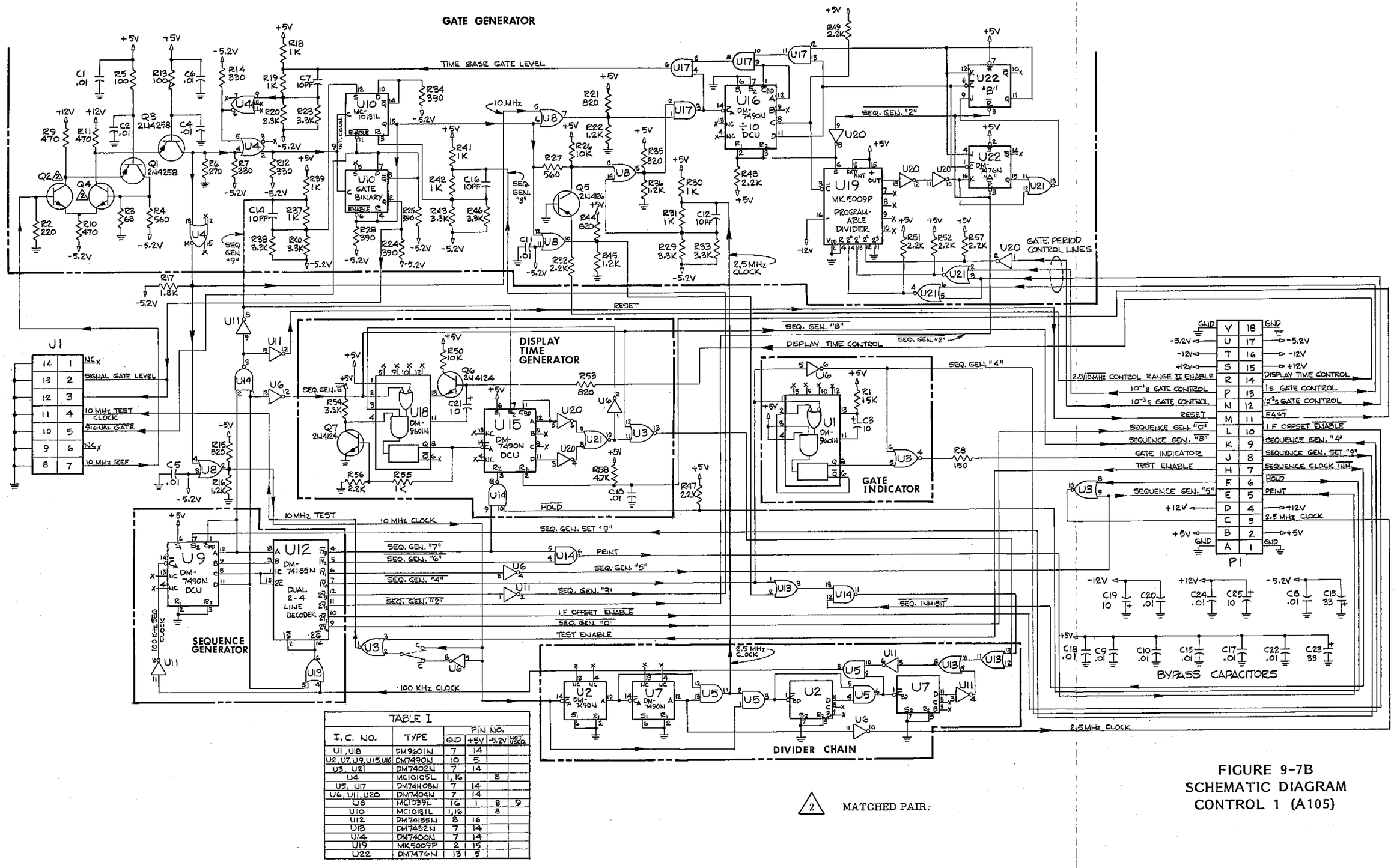
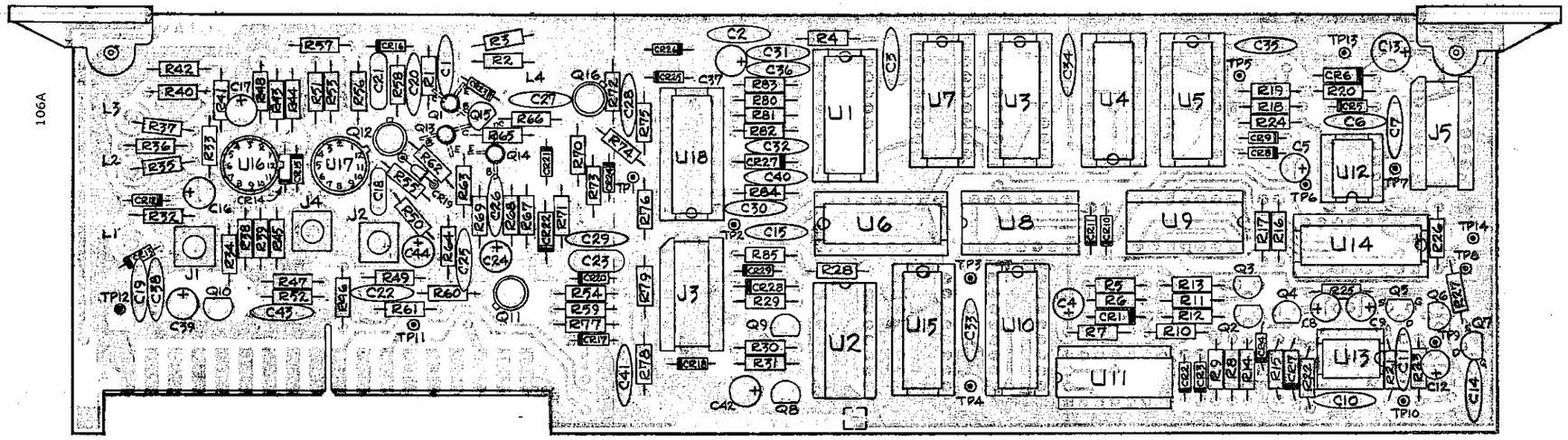


TABLE I					
I.C. NO.	TYPE	PIN NO. GND	+5V	-5.2V	NOT USED
U1, U18	DM9601N	7	14		
U2, U7, U9, U15, U16	DM7490N	10	5		
U3, U21	DM7402N	7	14		
U4	MC10105L	1, 16		8	
U5, U17	DM74H08N	7	14		
U6, U11, U20	DM7404N	7	14		
U8	MC1039L	16	1	8	9
U10	MC10181L	1, 16		8	
U12	DM74155N	8	16		
U13	DM7432N	7	14		
U14	DM7400N	7	14		
U19	MK5009P	2	15		
U22	DM7476N	13	5		

2 MATCHED PAIR.

FIGURE 9-7B
SCHEMATIC DIAGRAM
CONTROL 1 (A105)



HIGH FREQUENCY (A106)

The High Frequency board accepts RF signals from the Preamplifier (A111), Prescaler (A109), Converter (A2), gate and 10 MHz Test signals from Control 1 (A105). Range signals from Control 2 (A104) select the appropriate input which is processed, gated, and counted in the first decade counting unit (DCU). The outputs from A106 are the Carry (f/10) signal, and the first decade of BCD information. These signals go to Count Chain 3 (A103) for further processing.

High Frequency board A106 also provides programming, frequency division, phase comparison, integration, and part of the video signal amplification, for the source locking phase lock loop (PLL). All signals for the PLL portion of A106 enter or leave via J1, which connect to Microprocessor board A122.

Input Selector

A106 accepts three input signals (on J1, J2, and J4), and a 10 MHz Test signal (J3 pin 4). One of the three inputs is selected by a command signal entering on P1 pins 12, 13, or 14. Each command line sits at approximately -12 V until it is selected, at which time it is pulled up to about + 0.7 V. These command signals turn on an appropriate differential amplifier, which selects the input signal to be processed. The signal into each gated amplifier is terminated with a 51 ohm resistor.

If the input to J1 is selected, an additional amplifier stage (U16A) is also turned on by the control signal. This signal is ac-coupled into the preamplifier stage to allow the input to be biased at approximately -6 V. The collectors of U16A are operated against ground to minimize parasitics. L2 and L3 in series with load resistors R35 and R37, are high frequency peaking coils used to flatten the response of the amplifier. R36 is used partly as a damping resistor for L2 and L3, and partly to establish a -2 V level at the output of U16A for direct coupling to U16B. CR14 and CR15 prevent large signals from overloading U16B.

Squaring Circuits

The input selector differentially drives squaring circuit Q12 and Q19. Q12 is a current mirror which is used as a voltage-to-current converter. The current from Q12's collector is used to drive tunnel diode CR19. The action of a tunnel diode under a current driving signal is that of a Schmitt trigger; that is, the voltage across the diode changes abruptly between two states (approximately 0.1 and 0.5 V), and therefore changes a low frequency sine wave into a low frequency square wave, with rise and fall times on the order of half a nanosecond.

The voltage signal across the tunnel diode is used to drive the pulse forming network. The network input is a wide-band high speed differential amplifier (Q13/Q14), to increase the amplitude of the tunnel diode signal, and improve the rise and fall times. The output of Q13/Q14 drives current mirror Q15, used here as a current switch. Essentially, Q15 is either on or off, but the output is the current from the collector, and not a voltage signal. The switched current signal drives differentiator L4. The output of a differentiator with a square wave input is a series of pulses — positive when Q15 turns on, and negative when Q15 turns off. The negative pulses (wider than the positive pulses due to transistor storage time) are removed by CR23. Shorting out the negative pulses also provides a damping effect on L4, improving its response to the positive pulses at high frequencies.

Pulse Inverter

These positive pulses are then coupled to pulse inverter Q7, which has two functions: to invert the pulse, and to deliver the negative output pulses at the right dc reference level for decade divider U18. A temperature compensated stable dc reference is provided by voltage divider R75-77 and CR25-26. The inverter is kept from disturbing this reference by being biased just at cut-off. This is accomplished by developing a forward bias for the transistor from the voltage drop across CR14, whose voltage matches the base-emitter voltage of Q16, keeping Q16 just at the edge of conduction. Basically, Q16 is a pulse amplifier, since it only conducts during a signal pulse. The load resistor for Q16 is the net equivalent of the bias network R75-77.

Q16 output drives the input of decade divider U18. The divide-by-ten output of U16 is a 60/40% duty cycle ECL level signal, and is called the "DCU CARRY" signal (J3 pin 3); the load resistor for this signal is on A103.

The gate signal to the DCU is an inverted ECL signal. It enters on J3 pin 5, and goes directly to U18 pin 16. The BCD output information is available at J3 pins 1, 2, 13, and 14. During a count cycle at high frequencies, this information is slew rate limited, and actual output level cannot be seen until the circuit comes to rest. After the circuit is finished counting, TTL level signals are present at these outputs. U18 is reset after the counting cycle is complete by a TTL reset signal at pin 3.

Phase Lock Loop

The PLL generates a 50 kHz reference signal by dividing the counter's 10 MHz time base in the reference divider (U2B, U15A/B, Q8, Q9). The incoming 10 MHz signal is converted to a TTL signal by Q8 and Q9. The signal is then divided by two in U2, by ten in U15A, and by ten in in U15B, resulting in a total division of 200. The 50 kHz reference retains the same stability as the time base oscillator (A108). This reference signal is applied to phase detector U11 through phase reversing switch U10.

The second input to the phase detector circuitry comes from the frequency divider chain. The divider chain takes the IF frequency and divides it by the number programmed into it by frequency program registers U8 and U9. With the exception of two bits, the program number consists of four 4-bit numbers (in standard positive logic format), which correspond to the IF lock frequency.

The numbers are programmed serially into U8 and U9, with the parallel outputs programming the frequency divider chain (U3-U6) sequentially from the least significant digit to the most significant digit. Since the counter can never be programmed above 319.9 MHz, only two bits are required to program U5 (pins 5 and 11); the other two bits (pins 2 and 14) are hard-wired low. The two remaining bits from U9 are used for other programming functions: one bit (pin 10) is used to control the reversing of the reference and divided IF signals to change the polarity of the video signal; the other bit (pin 11) goes through J4 pin 1 to the Microprocessor board (A122) to select the narrow bandwidth mode of locking. (These last two functions, generated by the microprocessor on A122, have no correlation to the frequency being programmed.)

Phase Detector

The phase detector compares the phase of the two incoming signals by measuring the time difference between their leading edges. The output of phase comparator U11 consists of negative voltage pulses from pin 2 or pin 13, with the width of the pulses proportional to the phase error between the two signals. The advantage of this type of detector is significant when the two signals being compared are not the same frequency. When this occurs, the error pulses lengthen into a nearly dc signal, and the phase detector becomes a frequency comparator, indicating whether the divided signal is above or below the reference frequency. The only condition under which this type of phase detector can lock up, is when the two incoming frequencies are identical.

FIGURE 9-8A
COMPONENT LOCATOR
HIGH FREQUENCY (A106)

Charge Pump

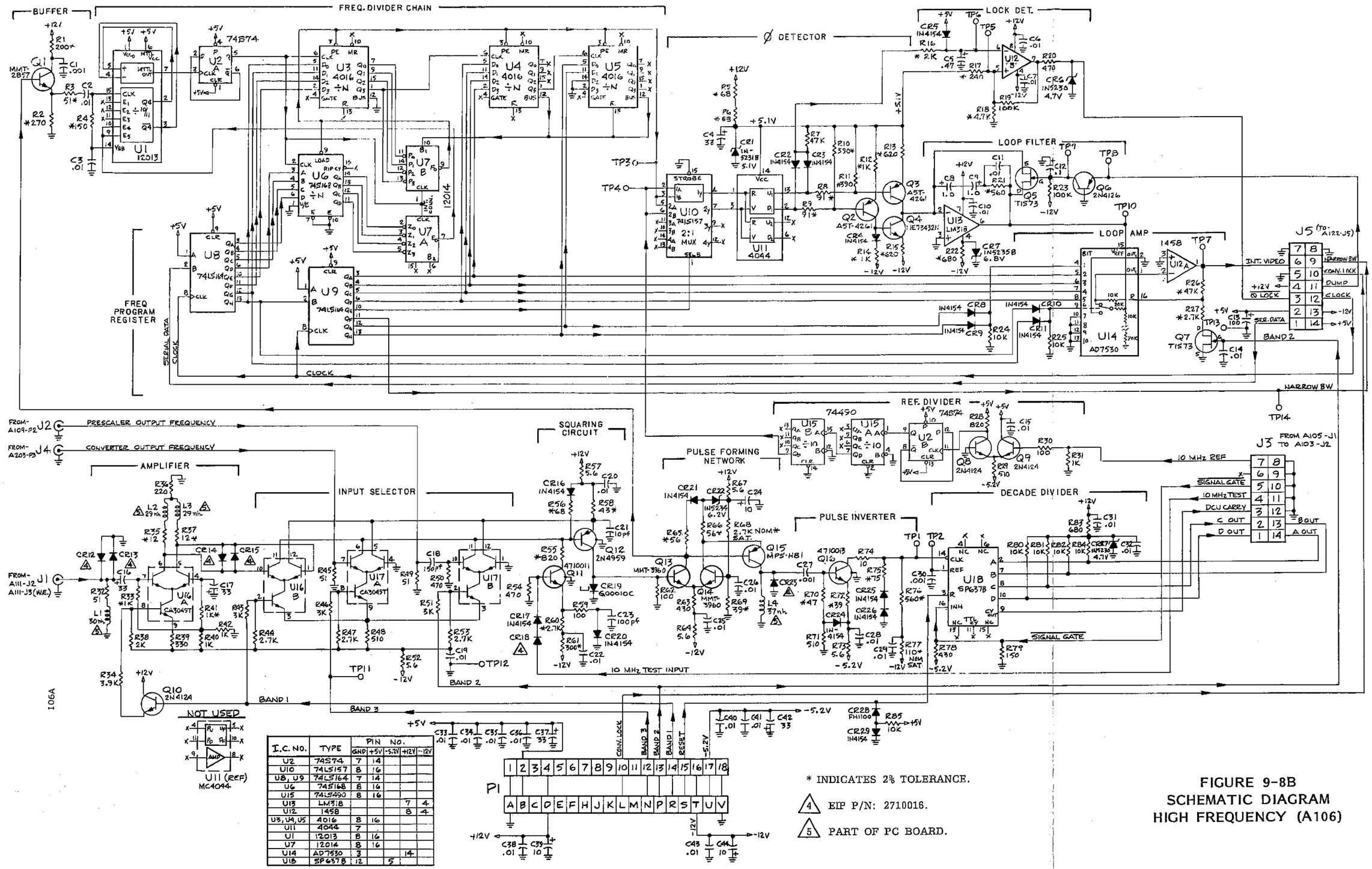
The remaining part of the phase detector circuitry (Q2 - Q4) is called the charge pump. This circuitry takes the voltage pulses from the phase comparator and converts them to current pulses. Q3 takes the negative voltage pulse from U11 (pin 13), and converts it to a 4.6 mA collector current pulse, at about the same width as the voltage pulse from U11. Q2 is an inverter which drives Q4, generating a 4.6 mA current pulse of opposite polarity to that of Q3. The current output pulses "pump" the charge across C8 and C9 in the loop filter up and down, to correct for the phase error between the two frequencies entering the phase comparator.

Loop Filter

The loop filter (Q5, Q6) is an integrating type, which has a dc gain equal to the open loop gain of amplifier U13. The gain of U13 decreases as a function of frequency, until the impedance of C8 and C9 is less than R21. Above this frequency, the output is equal to the input current times the value of R21. Since this is an integrating filter, capacitors C8 and C9 store a charge. At times during the lock up procedure, it becomes desirable to "dump" this charge. Q5 is held at cut-off by -12 volts applied to its gate. When current flows into Q6's emitter, Q6 saturates, and its collector and the gate of Q5, go to +0.2 volts. This turns on Q5, and dumps the charge on C8 and C9.

The output of the loop filter drives the loop amplifier, consisting of a DAC (U14) and an op amp (U12A). The DAC is a CMOS switching type that is used as a digital gain control. The gain in Bands IA, IB, and III, from TP10 to TP7, can be calculated from the equation: Frequency in MHz, divided by 70.

In Band II, the divide-by-four Prescaler requires that the gain of the loop amplifier be multiplied by four. This is accomplished by the Band II command signal turning on Q7, which switches R27 into the circuit. R27 essentially bypasses 3/4 of the feedback current, resulting in an increased stage gain of four. The output of U12A goes to A121 for further processing before being used to control the frequency of the source being phase locked.



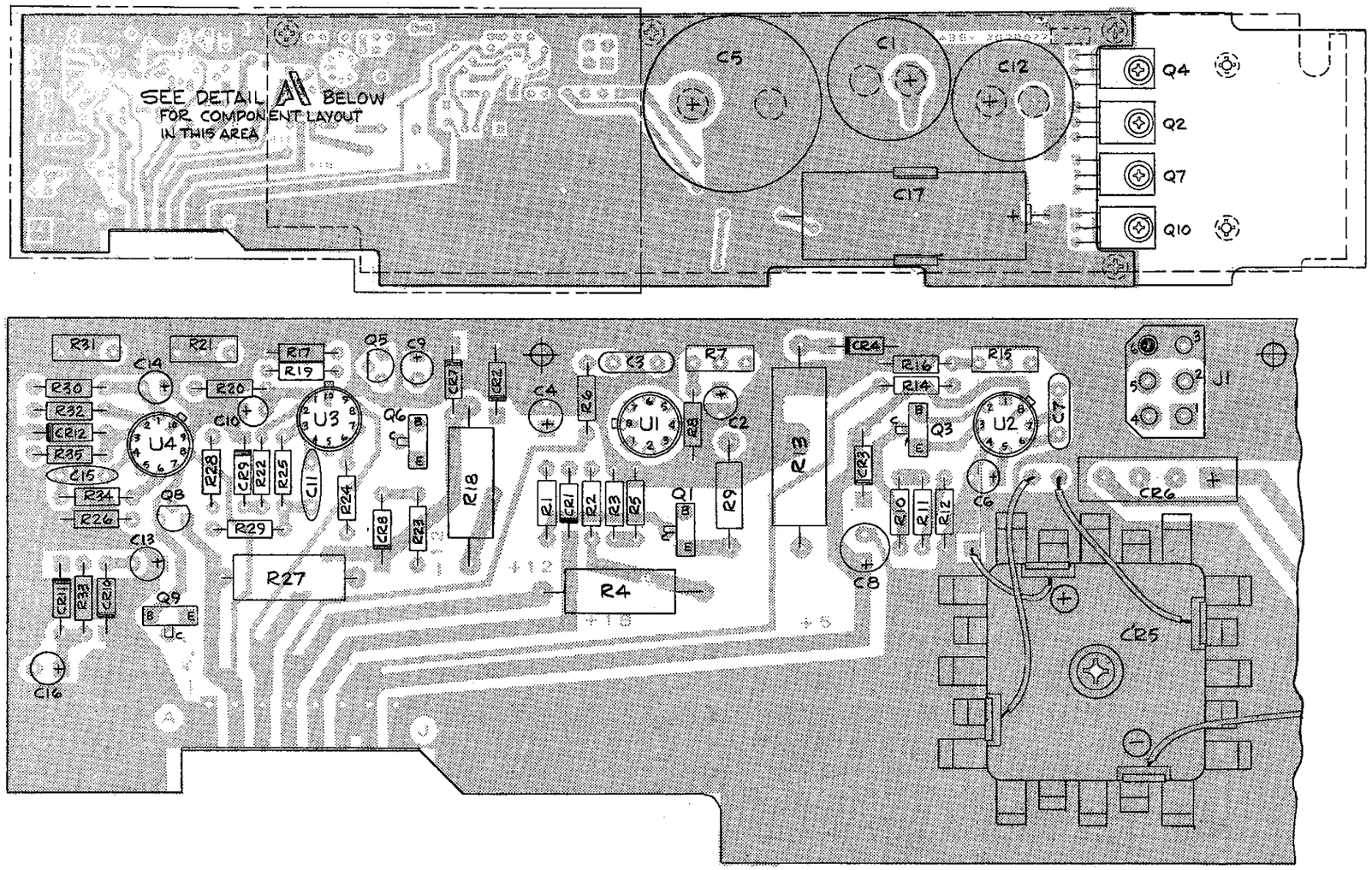
I.C. NO.	TYPE	PIN NO. GND	+5V	-5.2V	+12V	-12V
U2	74S74	7	14			
U10	74LS157	8	16			
U8, U9	74LS164	7	14			
U6	74S168	8	16			
U15	74S490	8	16			
U13	LM318				7	4
U12	1458				8	4
U3, U4, U5	4016	8	16			
U11	4044	7				
U1	12013	8	16			
U7	12014	8	16			
U14	AD7530	3			14	
U18	SP637B	12		5		

* INDICATES 2% TOLERANCE.

4 EIP P/N: 2710016.

5 PART OF PC BOARD.

FIGURE 9-8B
SCHEMATIC DIAGRAM
HIGH FREQUENCY (A106)



DETAIL A

POWER SUPPLY (A1/A107)

The Power Supply furnishes all basic operating voltages required by the counter. The supply consists of two assembly groups:

(1) PC Board A107 contains the rectifiers, filter capacitors, and regulator circuitry.

(2) Chassis mounted components (A1-) consist of the power transformer (T1), primary wiring, fuse (F1), 115/230 power switch (S102), and the front panel POWER On/Off switch (S101).

Circuit Description

The basic voltages that are required by the counter are: unregulated +18 V, regulated +12 V, -12 V, +5 V and -5.2 V.

All the regulated voltages are produced by full wave rectifier and series regulator circuits. The +18 V unregulated voltage is also the input voltage for the +12 V regulator.

Each of the four regulator circuits contains an integrated circuit voltage regulator with current foldback capability, protective diodes, and provision for adjustment of the required output voltage.

The type of IC used in both the +12 V and +5 V regulators is an LM305. This IC contains an internal temperature compensated voltage reference, as well as the necessary circuits to provide gain and current foldback limiting. The foldback current limit control resistors in the +5 V supply (for example) are R11, R12, and R13.

The negative supplies utilize an LM304 as the basic IC regulator. This IC also contains an internal temperature compensated reference. To implement this reference an external pre-regulator is required. In the -12 V circuit (for example), the pre-regulator includes R22, R25, and CR9. Current foldback limiting uses internal IC circuitry in addition to R17, R18, R19 and Q5.

FIGURE 9-9A
COMPONENT LOCATOR
POWER SUPPLY (A107)

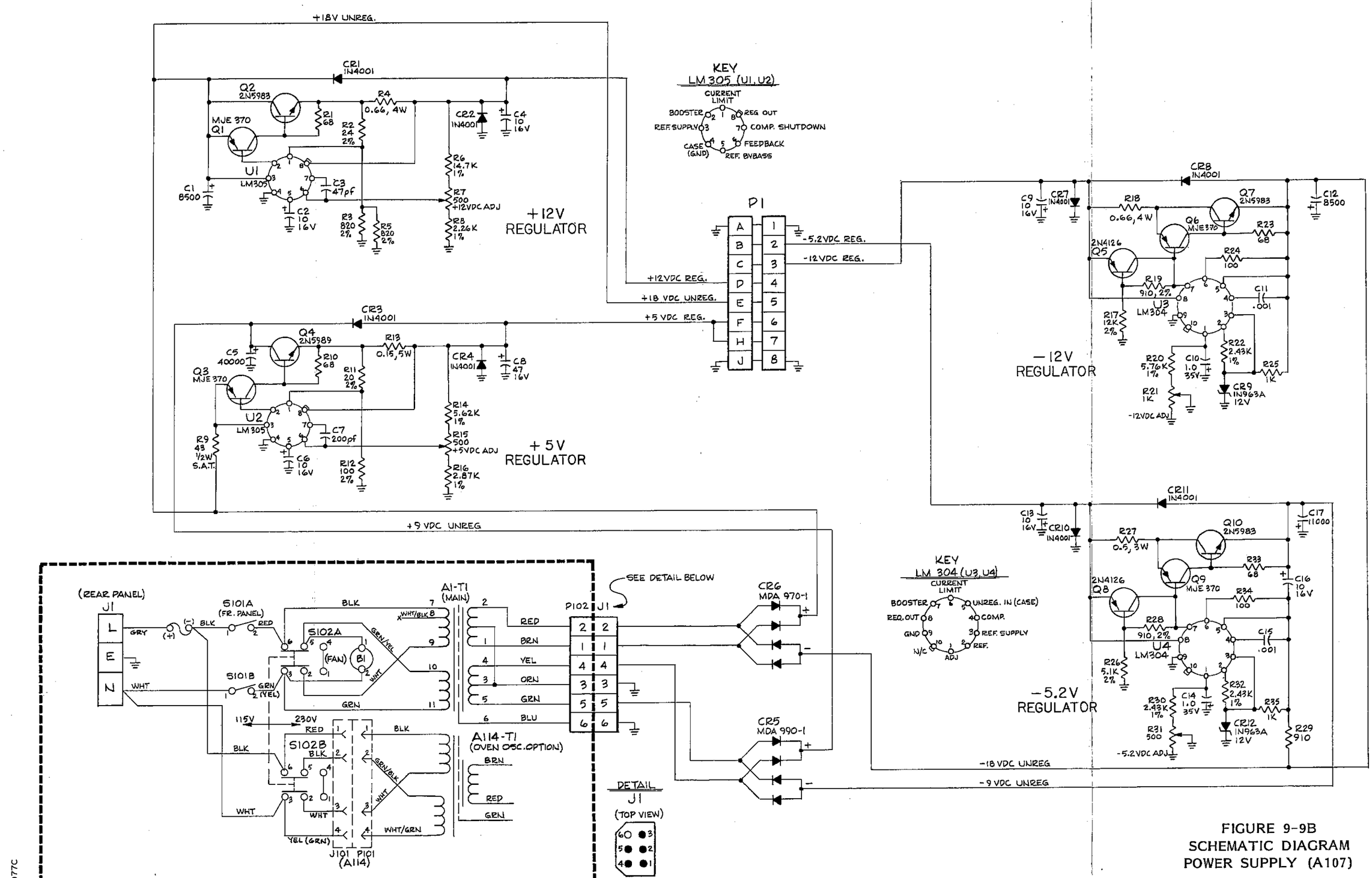
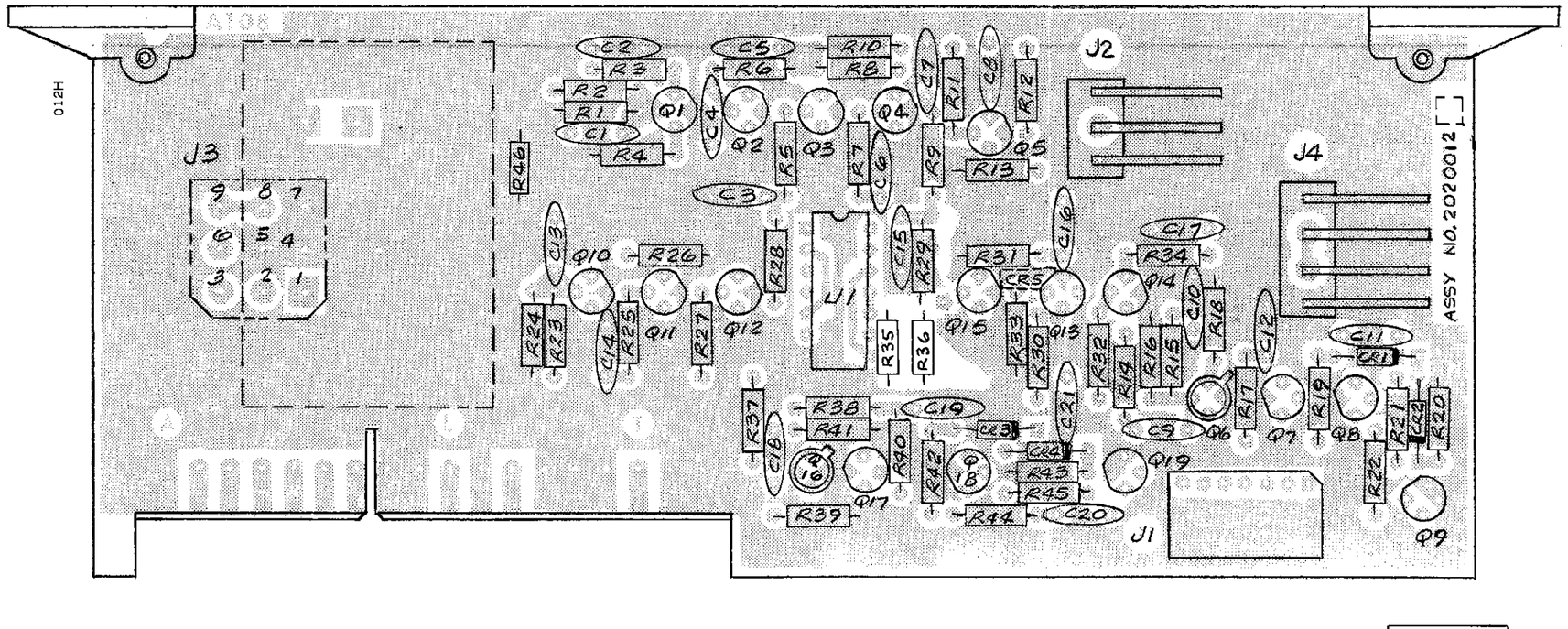


FIGURE 9-9B
SCHEMATIC DIAGRAM
POWER SUPPLY (A107)

077C



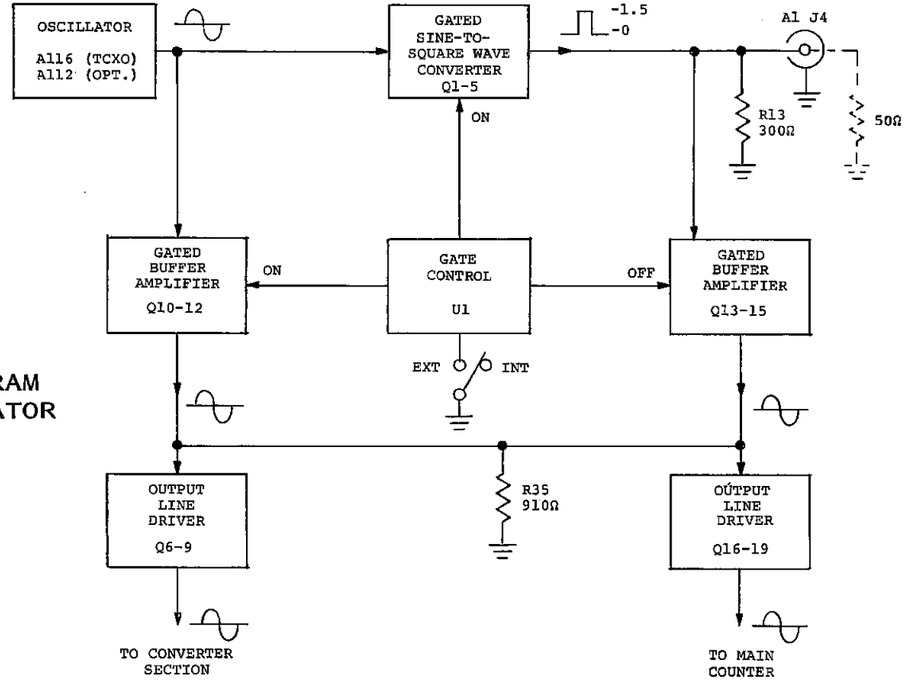


FIGURE 9-10C
FUNCTIONAL DIAGRAM
REFERENCE OSCILLATOR
BUFFER

REFERENCE OSCILLATOR BUFFER (A108)

An internal temperature-compensated crystal oscillator — TCXO (A116), is used as the basic reference against which all input signals are compared. Additional time base options are available (see Section O - Options), which allow the user to select a level of precision compatible with measurement requirements. Specifications of the TCXO are listed in Section 3.

The counter may be operated from either the internal time base oscillator (TCXO or oven option), or from an external time base reference generator. Internal or external selection is made by means of a rear panel switch (A1S103). A rear panel BNC connector (A1J4) connects to A108J2 to furnish a 10 MHz square wave output signal, or accept a 10 MHz sine or square wave input signal (1 to 3 V p-p into 300 ohms). The method of switching between internal and external oscillators is shown in the Functional Diagram of Figure 9-10C. The power to the TCXO is switched on and off with the main counter power supply, while the power to any of the oven oscillator options remains on as long as the counter is plugged into an active power line, irrespective of the setting of the POWER On/Off switch.

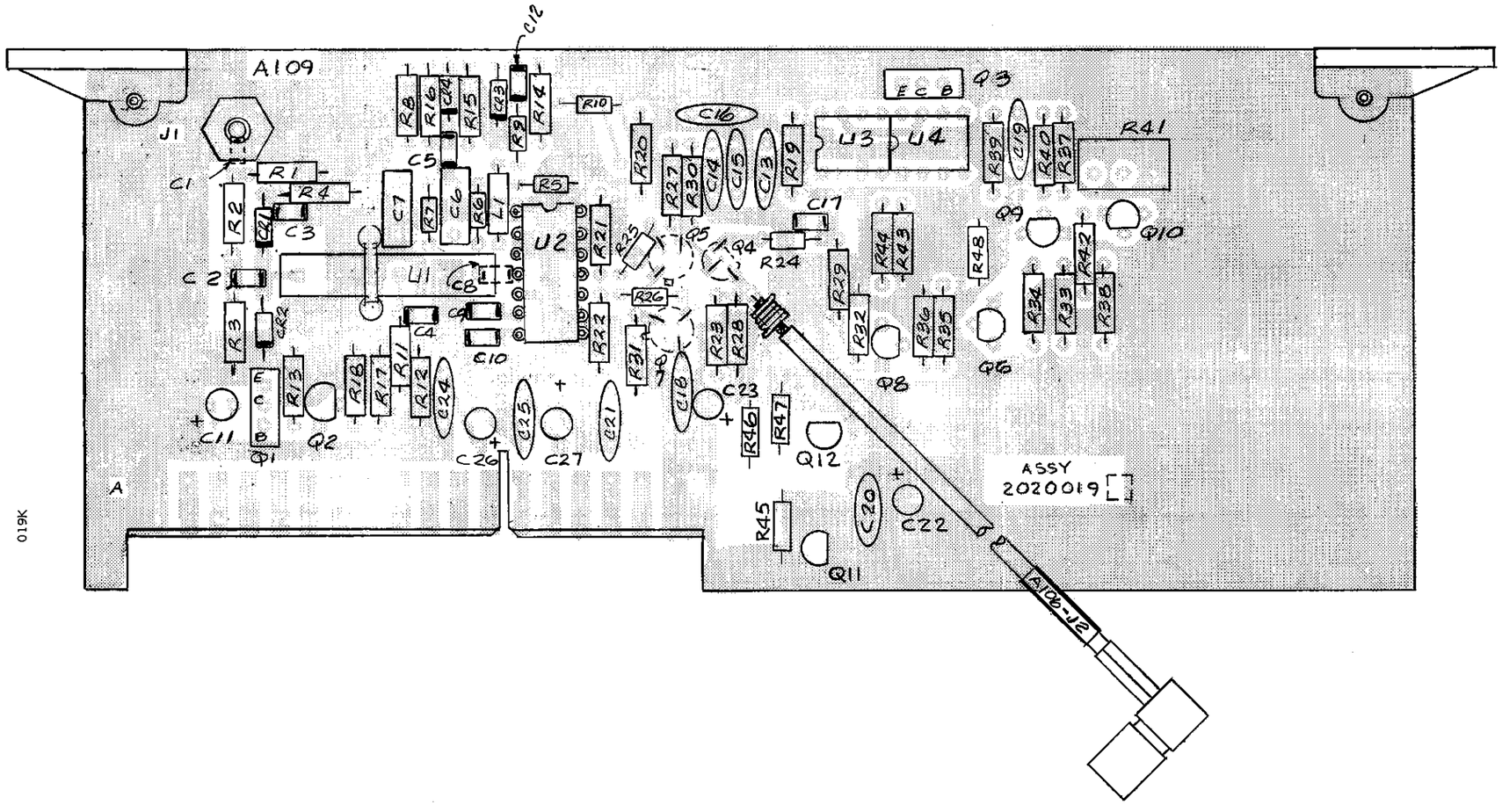
Circuit Description

The TCXO sine wave is gated and converted to a TTL level in the circuit consisting of: a linear, low-gain isolation amplifier Q1; a differential sine-to-square wave amplifier Q2 and Q4; and an output current driver Q5. The gate function is accomplished by switching Q3 on and off through U1. Transistors Q10 - Q12, and Q13 - Q15, are identical sets of gated buffer amplifiers. Buffered gain is obtained in each set by the low-gain NPN/PNP pairs Q10/Q11, and Q13/Q14. The gating function is performed by switching Q12 and Q15 on and off through U1. Q6 - Q9, and Q16 - Q19, are identical sets of output line drivers. Low-gain, common emitter input stages Q6 and Q16 are followed by emitter followers Q7 and Q17, which drive push-pull emitter follower output pairs Q8/Q9, and Q18/Q19.

FIGURE 9-10A
COMPONENT LOCATOR
REFERENCE OSCILLATOR
BUFFER (A108 + A116)

10 MHz OVEN. OSC. (A112) (OPTIONS 03, 04 OR 05)
J3-6
J3-3
J3-2
10K TIME BASE ADJ (REF. ONLY)
J3-8/9 +28V GND
J3-4/5/7
FREQ. SET AT 25°C
(A116)*
10 MHz OSCILLATOR
-12V
*NOT USED WITH OPTIONS 03, 04 OR 05
J3-1
R46 5
C1 .01
R1 8.2K
R2 3.9K
R3 390
C2 .01
Q1 2N3563
+5 VDC
C3 .01
R5 2K
C4 .01
R4 680
Q2 2N3563
R7 2.2K
C6 .01
Q3 2N3563
R8 750
R9 2K
R10 8.2K
Q4 2N3563
C7 .01
R6 8.2K
C5 .01
-12VDC
-5.2 VDC
+5VDC
R11 180
R12 27
Q5 2N4258
R13 300
C8 .01
+12 VDC
1 GROUND
2 TO 10MHz IN/OUT
3 GROUND
J2
R15 8.2K
C10 .01
R17 680
Q7 2N3563
Q6 4710011
R16 4.3K
R19 10
CR1 IN4154
CR2 IN4154
R18 560
Q8 2N3563
R21 5.1
R22 5.1
C11 .01
R20 1.1K
Q9 2N4258
C12 .01
+12 VDC
1 10 MHz OUT (TO CONVERTER INTERCONNECT A208)
2
3
4
J4
C9 .01
R14 10
10 MHz
+12 VDC
10 MHz
+12 VDC
R23 10K
R25 620
R27 430
C14 .01
C13 .01
Q10 2N3563
Q11 2N4258
R24 2K
R26 300 5
R28 2.2K
Q12 2N3563
U1 DM74D1N
+5 VDC
R29 5.1K
C15 .01
R30 8.2K
R32 620
C16 .01
Q13 2N3563
Q14 2N4258
R34 430
C17 .01
CR5 IN4154
R31 3.6K
R33 360
R35 910
Q15 2N3563
+12 VDC
R36 2.2K
R37 10
C18 .01
R39 4.3K
R38 8.2K
C19 .01
R40 680
Q16 4710011
Q17 2N3563
R41 560
R42 10
CR3 IN4154
CR4 IN4154
R43 1.1K
Q18 2N3563
R44 5.1
R45 5.1
C20 .01
Q19 2N4258
C21 .01
+12 VDC
J1
10 MHz OUT (TO CONTROL I-A105)
012E
Q1- Q19 KEY
(BOTTOM VIEW)
2N3563
2N4258
4710011
CASE
E
C
B
5 VALUE SELECTED AT TEST. PART MAY NOT BE USED.
J3
J3 USED WITH OPTIONS 03, 04, OR 05 ONLY.
A 1 GROUND
B 2 -5.2 VDC IN
C 3 -12 VDC IN
D 4 +28 VDC IN
E 5 TIME BASE ADJ. POT.
F 6
H 7
J 8 GROUND
K 9
L 10 +5 VDC IN
M 11 GROUND
N 12 INT
P 13
R 14 GROUND
S 15 EXT
T 16 +12 VDC IN
U 17
V 18 GROUND
TIME BASE (REF. ONLY)
OPTIONS 03, 04 AND 05 ONLY
P1

FIGURE 9-10B
SCHEMATIC DIAGRAM
REFERENCE OSCILLATOR
BUFFER (A108 + A116)



PRESCALER (A109)

This assembly permits the measurement of frequencies in the range of 100 MHz to 850 MHz, dividing the input frequency by a factor of four prior to counting. The counter then counts this scaled frequency with a gate time which has been expanded by four, thus yielding a direct frequency readout.

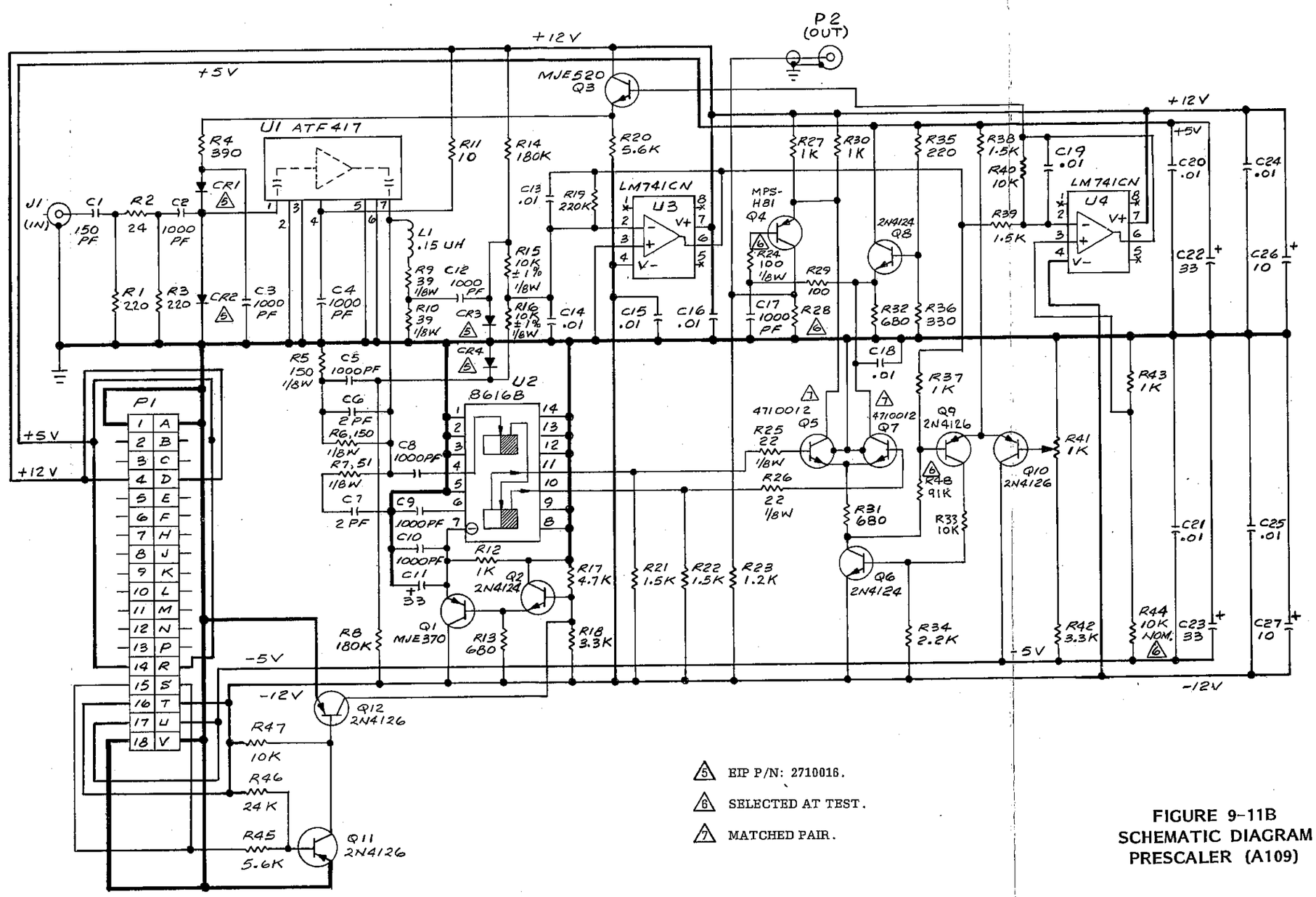
The major element of A109 is a ÷4 integrated circuit (U2). Sufficient drive level for this IC is provided by an integrated broad band amplifier U1. The output of U2 is amplified by the circuit consisting of Q4 through Q8.

Due to the tendency of U2 to free run with no input signal, it is necessary to disable the output if an input signal of sufficient amplitude is not present. This is accomplished with a threshold circuit consisting of a detector (CR3, CR4 and associated components), amplifier (U3), and differential trigger (Q9 and Q10). When the amplifier output applied to the base of Q9 exceeds the threshold level set by R41, Q9 turns on Q6 and thus enables the output amplifier.

In order to prevent U1 from overloading, automatic gain control is provided by comparing the amplified detector output to a preset level in U4 and feeding the output level back via Q3 to a pair of diodes CR1 and CR2. These diodes, when conducting, act to attenuate the input signal.

Transistors Q1 and Q2 form a -7 volt power source for U2.

FIGURE 9-11A
COMPONENT LOCATOR
PRESCALER (A109)



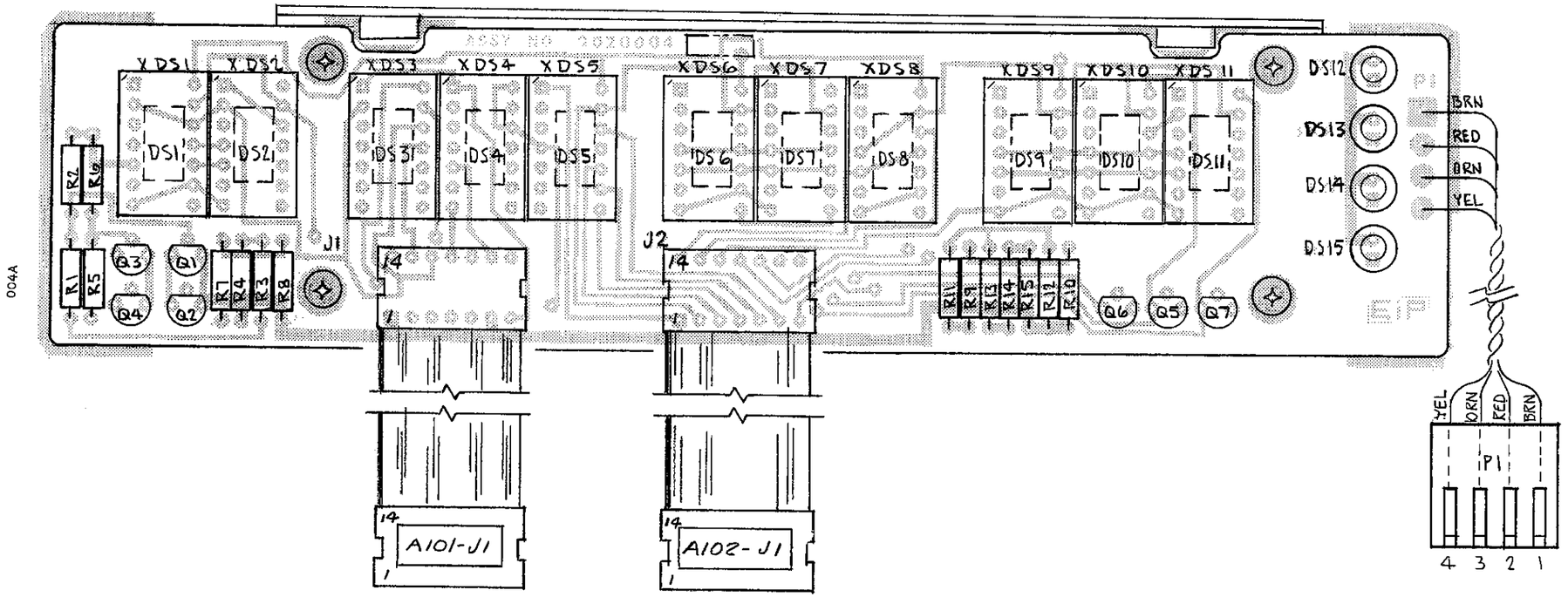
5 EIP P/N: 2710016.

6 SELECTED AT TEST.

7 MATCHED PAIR.

H610

FIGURE 9-11B
SCHEMATIC DIAGRAM
PRESCALER (A109)



DISPLAY (A110)

The Display Board (A110) contains eleven LED numerical display units mounted side-by-side, with spaces between each third digit from the right. The entire assembly is mounted behind a front panel window with the digits grouped to distinctly show GHz, MHz, kHz, and Hz. All drive signals for the Display are obtained from the Count Chain Boards (A101 and A102).

The digit displays are 7-segment LED's, with the anodes of each segment tied together. When the anode is at a positive voltage, grounding any cathode through its resistor illuminates that segment.

In this multiplexed system, the anode supply is applied in pulses (through anode drivers), which are synchronized with the cathode data to determine which segment shall light.

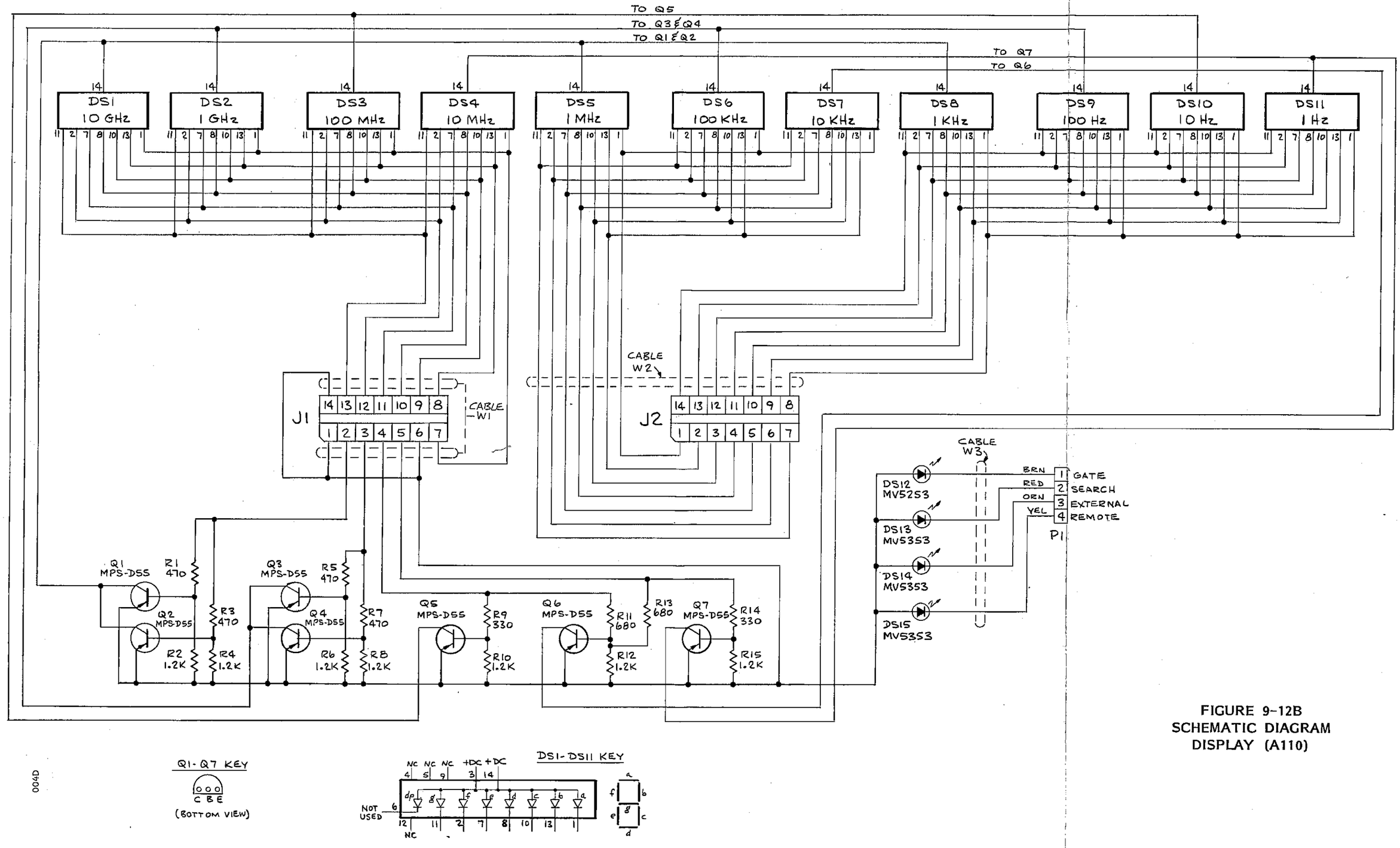
The segment drive is applied directly to the display digits. DS1-4, DS5-7, and DS8-11 have their corresponding cathode segments tied together within each group.

The selector drive to groups DS1, -5, -8, and DS2, -6, -9, are each driven by two transistors in parallel to meet the higher current requirements.

The remaining LED's use single transistor drivers. The drivers saturate when turned on, applying a voltage almost equal to the supply voltage for the display. This voltage is variable (by A103R22) for display brightness adjustment.

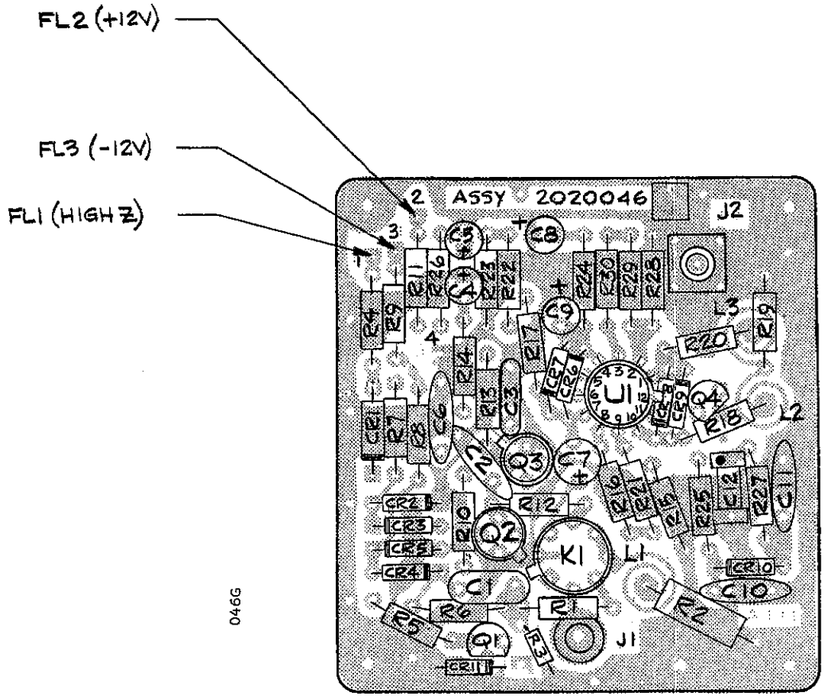
Four display lamps are included on this assembly, which illuminate to indicate GATE operation, Converter SEARCH, EXTernal REFerence, and REMOTE operation (Option 07).

FIGURE 9-12A
COMPONENT LOCATOR
DISPLAY (A110)



004D

FIGURE 9-12B
SCHEMATIC DIAGRAM
DISPLAY (A110)



PREAMPLIFIER (A111)

The Preamplifier accepts Band I input signals at J1. The BAND SELECT switch controls relay K1 which selects either the Band IA high impedance (1 meg/20 pf) circuitry, or the Band IB low impedance (50 ohm) circuitry. The output of the Preamplifier (at J2) drives the High Frequency Board (A106).

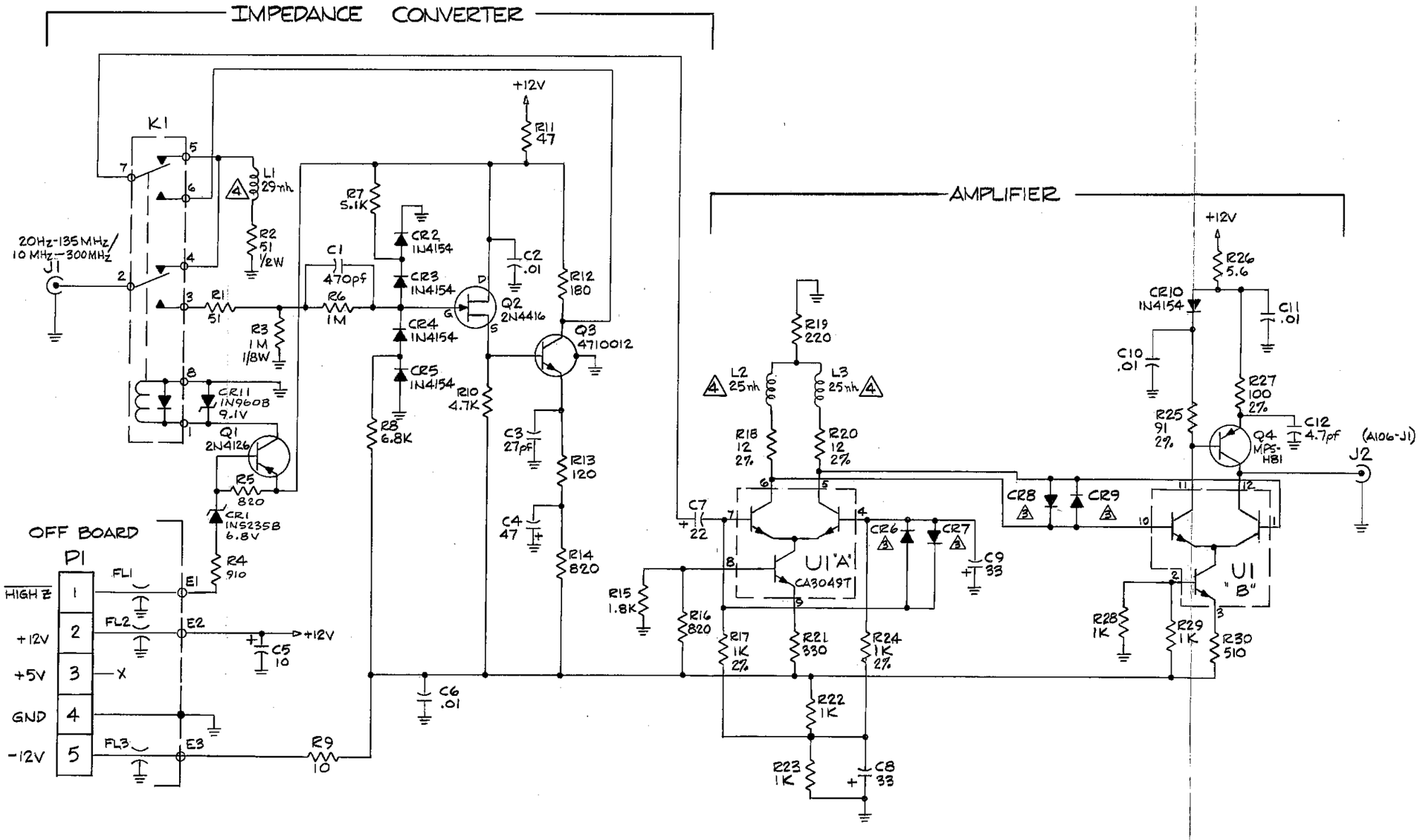
When K1 is de-energized, the amplifier operates in the 50 ohm mode. The terminating impedance is the parallel product of a 51 ohm resistor (R2) in series with a small inductance (L1), and the input impedance of the first amplifier stage (U1A). This combination keeps input VSWR below 1.5:1 up to 400 MHz. The signal is ac-coupled thru C7 to amplifier U1A, which is biased at approximately -6 Vdc. The collectors of U1A are operated against ground to minimize parasitic problems. Inductors L2 and L3 in series with load resistors R18 and R20, are high frequency peaking coils to flatten the response of the amplifier. R19 is used primarily to establish a dc voltage sufficiently negative to allow direct coupling to the second stage (U1B).

The output of the second stage is also operated against a ground reference. U1B pin 11 output is fed into current mirror Q4, whose output is then summed with the current of U1B pin 12, at J2. In this way, the two currents cancel, and only a small error component is left to generate an off-offset at the load.

When K1 is energized, the amplifier operates in the high impedance mode, with the relay routing the input signal to the impedance converter. The input impedance of the converter is essentially R3 in parallel with a network of components, and the gate of FET Q2. The net impedance of this combination is 1 megohm shunted by about 20 pf. The signal enters the gate of Q2 through diodes CR3 and CR4, which provide protective limiting for Q2. The limiter diodes are back-biased at about 0.7 V by networks R7/CR2 and R8/CR5. This back-biasing improves the frequency response by reducing the capacitance of CR3/CR4. The limiter is adequate to protect against an accidental connection of a 115 V, 60 Hz power line to the input, however, due to frequency compensating capacitor C1, this high voltage tolerance decreases as the frequency increases (see Specifications).

Q2 operates as a source follower to transform the impedance down to several hundred ohms. Q3 is a buffer amplifier with a gain of about 1.5; its purpose is to match the output of Q2 to the input of amplifier U1A, and to recover the loss of Q2 gain. The net gain through the Preamplifier is approximately equal for both high and low impedance inputs.

FIGURE 9-13A
COMPONENT LOCATOR
PREAMPLIFIER (A111)

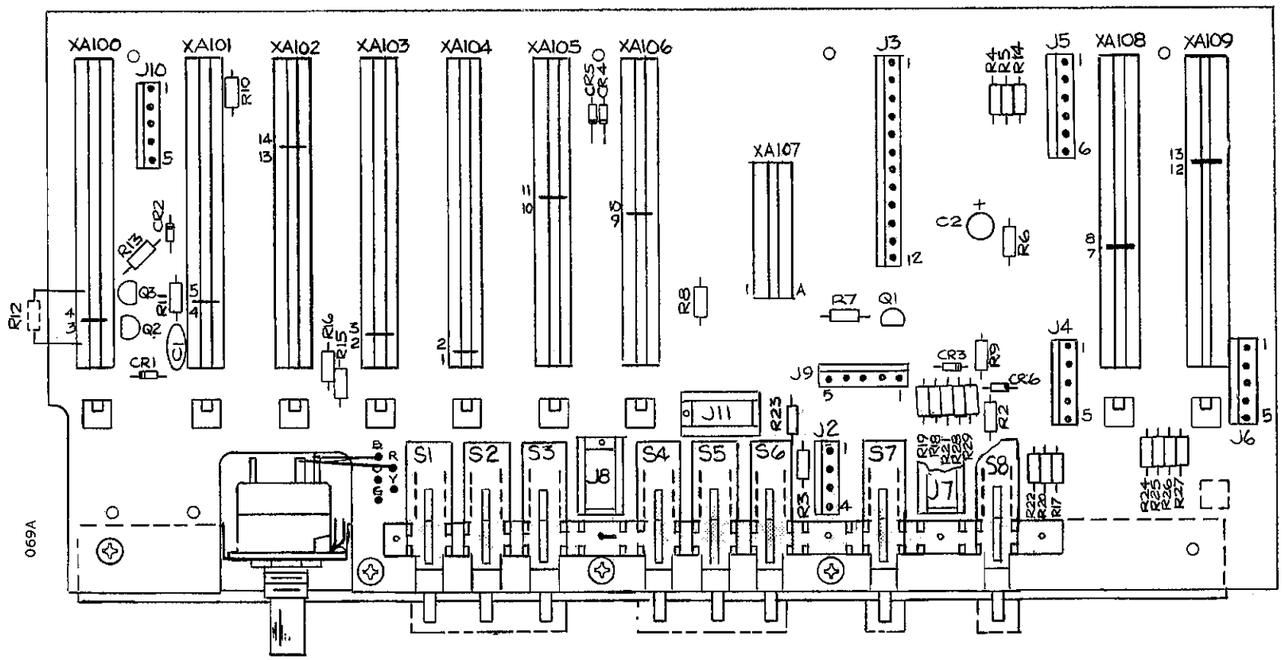


3 P/N: 2710016.

4 INDUCTOR PART OF PC BOARD.

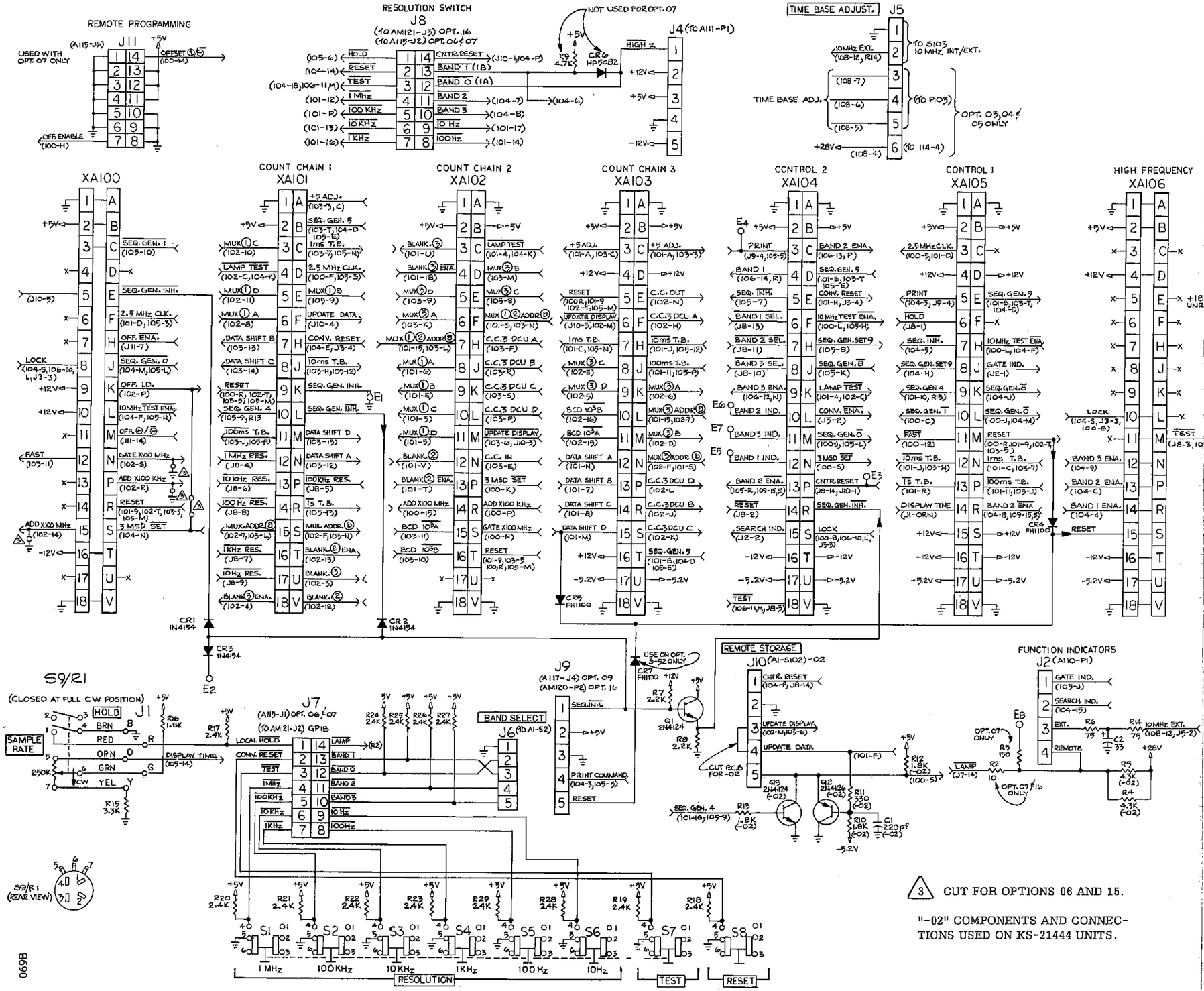
FIGURE 9-13B
SCHEMATIC DIAGRAM
PREAMPLIFIER (A111)

046E



NOTE: COMPOSITE PCB ASSEMBLY.
CERTAIN COMPONENTS USED ONLY
FOR SPECIFIC OPTIONS AND MODELS.

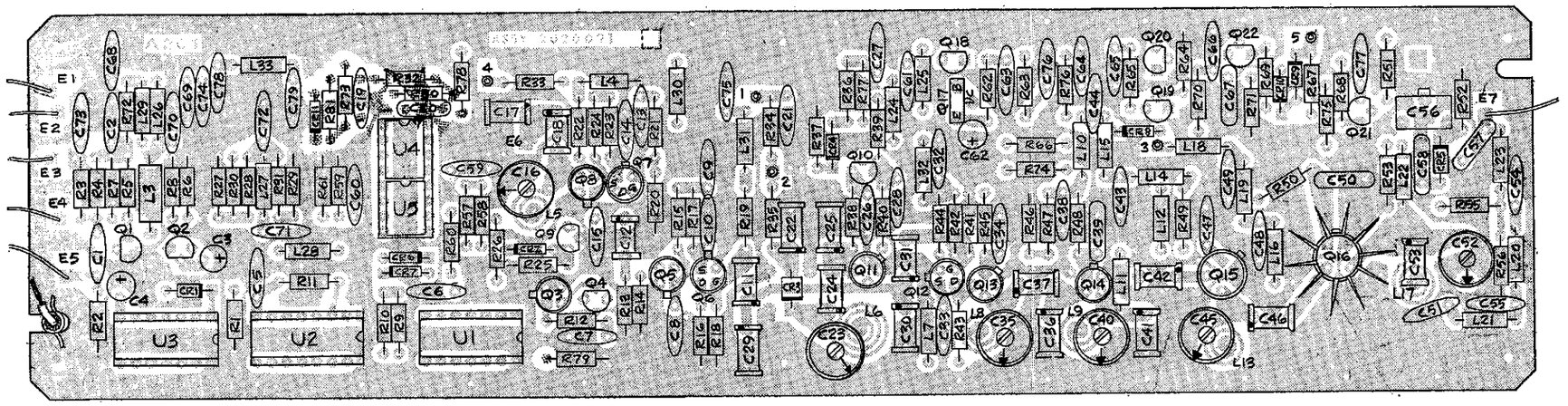
FIGURE 9-14A
COMPONENT LOCATOR
COUNTER INTERCONNECT (A113)



3 CUT FOR OPTIONS 06 AND 15.

"-02" COMPONENTS AND CONNECTIONS USED ON KS-21444 UNITS.

FIGURE 9-14B
SCHEMATIC DIAGRAM
COUNTER INTERCONNECT (A113)



91K60

SOURCE AMPLIFIER (A201)

General

A source of up to one watt of power at 200 MHz is required to drive the step recovery diode Comb Generator in YIG module A207. The 200 MHz must be both stable and coherent with the master oscillator in the counter. Stability is required to provide an IF spectrum that is dependent only upon the input signal spectrum. Coherence with the master oscillator is required to make counting accuracy dependent only upon the accuracy of the master oscillator.

The requirements of stability and coherence are satisfied by using a phase locked loop to lock a 200 MHz LC oscillator to the 10 MHz Time Base oscillator. The required output power is generated by a class C amplifier that contains a leveling loop to set the power output at any desired level from 1 mw to 1.1W.

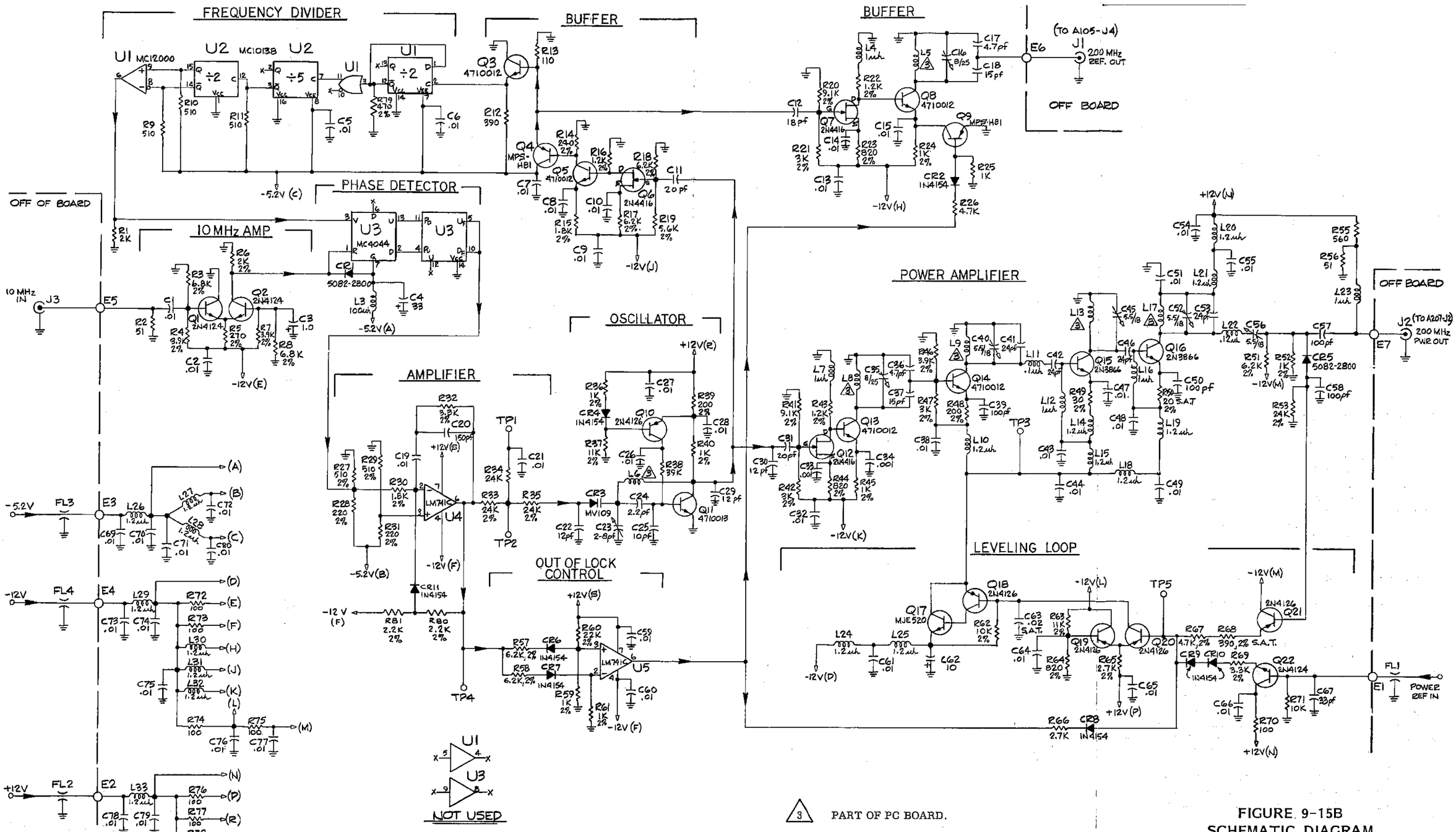
Circuit Description

The phase lock loop is a standard second order loop, implemented by using digital phase lock loop components. The 200 MHz LC oscillator is a modified Colpitts circuit with bias stabilization supplied by Q10. The output frequency of the 200 MHz oscillator is divided by 20 in U1 and U2 to produce a 10 MHz square wave. This signal is compared to the processed 10 MHz reference by phase detector U3. Phase error is amplified by active filter U4 and applied to voltage variable capacitor CR3. This holds the 200 MHz oscillator "locked" in phase to the 10 MHz reference signal. C23 sets the open loop center frequency of the oscillator.

The main power amplifier consists of four stages: Buffer amplifier Q12 and Q13, linear amplifier Q14, and two Class C stages Q15 and Q16. Output power level is controlled by adjusting the value of the negative voltage supplied by Q17 and Q18 to the linear amplifier and the Class C stages.

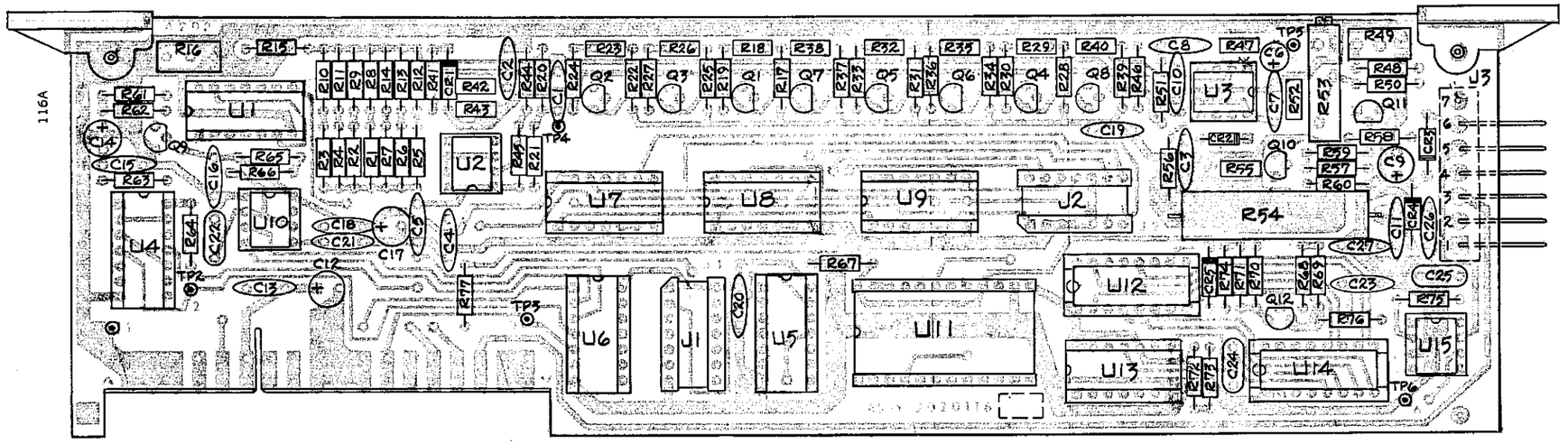
The power leveling loop operates by sampling the peak value of the output signal with CR5, and comparing this value to the Power Reference. The comparison is made by differential amplifier Q19 and Q20, which then controls Q17 and Q18.

FIGURE 9-15A
COMPONENT LOCATOR
SOURCE/AMPLIFIER (A201)



3 PART OF PC BOARD.

FIGURE 9-15B
SCHEMATIC DIAGRAM
SOURCE/AMPLIFIER (A201)



CONVERTER CONTROL 2 (A202)

Converter Control 2, utilizing enable and reset commands from Converter Control 1 (A203), creates the signals required to tune the frequency of the YIG Comb Generator, and control its output power. A202 consists of three principal circuits: DAC 1 and DAC 2, which provide a linear control voltage for the YIG sweep; the YIG Driver, which converts the linear outputs of the DACs to the proper drive currents for the YIG; and the Power Leveler, which controls the YIG output current.

Digital-to-Analog Converter Section

This section consists of a clock generator, DAC 1 (the main DAC), DAC 2 (the fine DAC), and the DAC control circuitry. U10 generates pulses at a 500 microsecond rate. These pulses drive either DAC 1 or DAC 2. If DAC 1 is enabled, the clock drives U7-9, whose outputs go to transistors Q1-8. When the appropriate output goes high it saturates the transistor, effectively connecting the collector resistor to the temperature compensated 3.1 V reference. This sums current into U3A causing the output to step up in voltage. The linear step function is achieved by properly selecting the values of the collector resistors for Q1-8. The high precision of these resistors, and the stability of the 3.1 V reference, provides the needed accuracy. Because the A output of U7 does not drive the sum line, the speed of DAC 1 is effectively divided-by-two, giving it a rate of 1 ms/step. The amplitude of the DAC is equivalent in YIG current to 200 MHz/step. The outputs of U7-9 are also connected to J2, providing the 3MSD information to the Count Chain.

In DAC 2, the clock drives U1 whose outputs are connected directly through resistors to the sum line. Because of the small size of DAC 2 (1.5 MHz/step), the accuracy of DAC 1 is not needed. Q9 provides a backward step at the beginning of DAC 2 to compensate for eddy current delays within the YIG Comb Generator.

Sweep Driver Section

The Sweep Driver section consists of an operational amplifier, a voltage translator, and two cascaded output transistors. The second output transistor (A2Q1) is located on the Converter chassis.

The ramp from the DACs drives the inverting input of U3B; R49 sets the ramp offset, and R53 determines the slope of the ramp. Feedback voltage is obtained across sense resistor R54, forcing an extremely linear relationship between the sweep voltage and the YIG filter current. CR3 limits the voltage developed across the YIG filter tuning coil during flyback, to protect Q11 and A2Q1.

Power Control Section

The Power Control section consists of an E PROM (U11), and a binary DAC (U14, U15). The 3MSD lines drive the address inputs of U11, which generates, for each address, the proper buffered 8-bit output which feeds the input of the 8-bit DAC. The analog output of the DAC is the signal which controls the YIG comb power by adjusting the output power of the Source Amplifier (A201).

During Reset, or when the Converter is not enabled, Q12 and U13B effectively cut the reference current in U14 to zero, thus shutting down the power level output.

FIGURE 9-16A
COMPONENT LOCATOR
CONVERTER CONTROL 2 (A202)

I.C. NO.	TYPE	GND	+5V	+12V	-12V
U4	7400	7	14	—	—
U5-U6	7404	7	14	—	—
U13	7408	7	14	—	---
U11	1702A	AS SHOWN			
U12	MC14050	8	1		
U7-U8-U9	74176	7	14	—	—
U1	74393	7	14	—	—
U15	LM741	—	—	7	4
U14	MC1408L-6	AS SHOWN			
U2-U3	MC1458	—	—	8	4
U10	NE555	1	8	—	—

NOT USED

7404 U5C

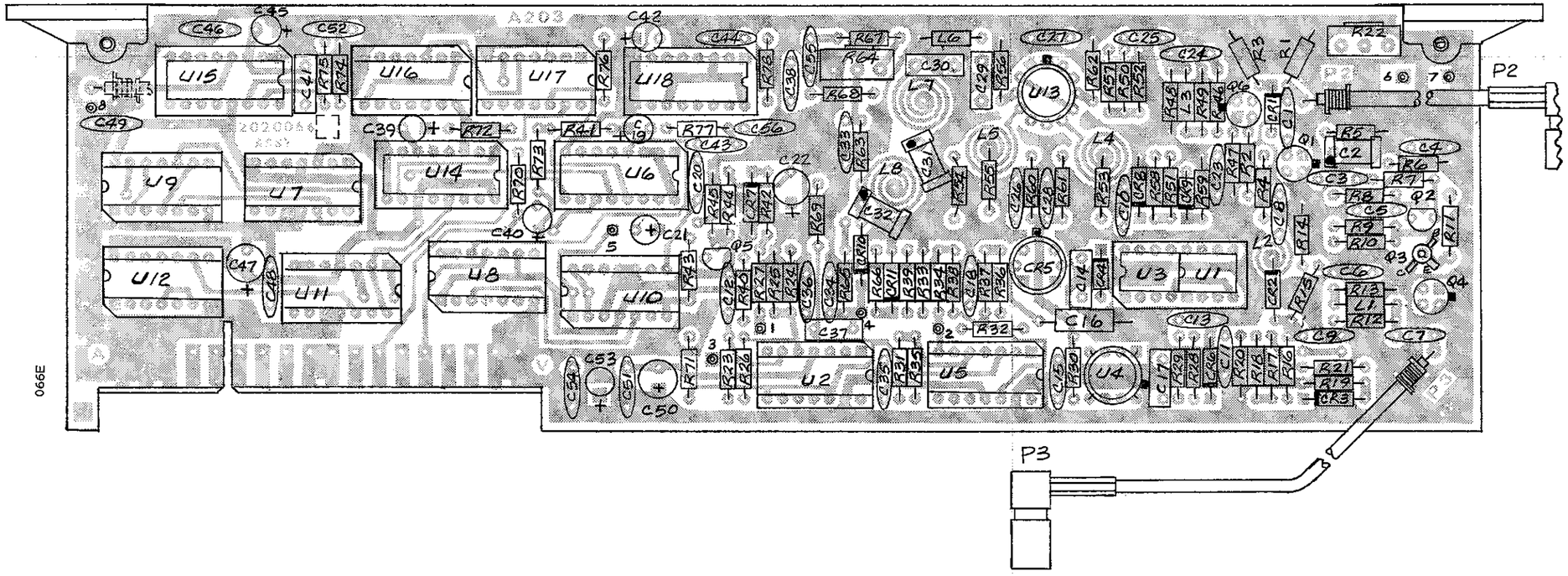
7408 U13A

3 J1, J2 NOT USED ON 371 COUNTER.

4 P1-D/4 CONNECTS TO A208P1-14.

FIGURE 9-16B
SCHEMATIC DIAGRAM
CONVERTER CONTROL 2 (A202)

116A



CONVERTER CONTROL 1 (A203)

Converter Control 1 performs all the control functions necessary to lock the microwave Converter to the correct YIG/Comb Generator (A207) output frequency, and provide appropriate signals to the direct counter.

Converter Control 1 consists of five basic functional sections: a Video Limiter, a Video Detector, an In-Band Detector, an Analog Processor, and Signal Acquisition Logic. The Video Limiter processes the signal from A204 to provide a constant amplitude signal to the High Frequency board (A106). The Video Detector converts the incoming video signal from A204 to a level proportional to the incoming power. This signal is then compared to a number of preset levels in the Analog Processor circuits, and converted into digital signals for further processing. The In-Band Detector is used to determine whether or not the video frequency falls within the desired passband, and to enable the Analog Processor circuits. The Signal Acquisition Logic provides the digital commands to control the sweep circuits and to lock the Converter on the appropriate comb line.

Figure 9-17C shows the operating sequence of the Converter. In the absence of an input signal to the Converter, a 200 MHz/ms sweep is continuously generated (DAC 1 ENABLE and CLOCK ENABLE are high). At the end of each sweep, a CONVERTER RESET command is generated (point A to point B on waveform). When a signal is applied, a Video Detector output will be generated when the YIG filter is tuned through the correct harmonic (point C). When this signal appears, a CONVERTER RESET command is again generated (point C to point D), and the sweep is reset to zero. A new sweep is initiated (point D) and eventually the Video Detector again produces an output (point E). At this point, a small backward step will be taken, followed by a 3 millisecond delay (point E to point F). At the end of this time, DAC 2 turns on, and a considerably slower sweep (4 MHz/msec) begins. At point G, the Video Detector output has reached 90% of the value stored in the Peak Detector, and the sweep is stopped. Three milliseconds later (point H), a LOCK command is given, which will allow the counter to read the frequency applied to the High Frequency board (A107). If the sweep is inhibited from stopping at point G (by grounding A203TP4), the Video Detector output will appear as shown by the dotted line on the waveform.

Video Limiter and Video Detector Sections

The incoming signal from the Video Amplifier (A204) enters at connector P2, passes through an isolation buffer Q1, and is limited by the differential amplifier Q2-Q4. This provides a fixed output amplitude of approximately 1 V peak-to-peak to the High Frequency board. Q1 also drives Video Detector diode CR2. Diode CR3 (matched to CR2) is used for temperature compensation of CR2 bias. The rectified signal is then amplified by U31, whose gain is set by Video Detector Gain Control R22. The setting of R22 determines the minimum required lock signal from the Video Amplifier. As such, its setting plays an important part in determining the sensitivity of the Converter. Refer to Section 6 for the proper adjustment procedure.

In-Band Detector

The Video Amplifier also drives an additional buffer Q6, which provides the drive signal for a two-stage limiter U13. This limiter drives a bandpass filter, whose output is then detected by CR10. (Matched diode CR11 provides temperature compensation for CR10.) The output level of CR10 is thus a function of frequency only. When the output of CR10 exceeds the DC level set by R21, the In-Band Detector triggers, generating a TTL compatible output signal. Trigger level hysteresis prevents the In-Band Detector from turning off until the signal is reduced considerably in power. R64 is set to turn on the In-Band Detector at 250 MHz. Once turned on, it will not turn off until the frequency is increased to approximately 275 MHz. It is this difference in turn-on and turn-off frequency which determines the FM tolerance of the heterodyne Converter at the edge of the video passband.

During Reset time the YIG/Comb Generator has no output, so no in-band should be generated. If one is generated, it is an indication that the input to the Converter contains spurious signals of sufficient amplitude to interfere with the operation of the in-band. The Noise Control circuit senses this in-band and generates a ramp to increase attenuation of the input signal via the PIN Diode Attenuator (A206) until in-band goes away, at which point the spurious inputs no longer create a problem. After Reset, A206 remains preset to that amount of attenuation, and the Converter can function with no interference from spurious signals.

Analog Processor

The Analog Processor contains a DC-coupled comparator, and a Peak Detector. The purpose of this section is to convert the analog output of the Video Detector into digital commands which can be used to lock the Converter to the correct comb line. U2A compares the Video Detector output to preset levels, and is used to determine that there is sufficient power level from the Video Amplifier. This comparator is enabled by the In-Band Detector output.

Operational amplifiers U3, U4, and associated circuitry, form a Peak Detector which stores the maximum Video Detector output during a particular sweep period. U5A compares the stored output of the Peak Detector with the instantaneous value of the Video Detector output. Switching occurs when that output reaches 90% of the stored peak.

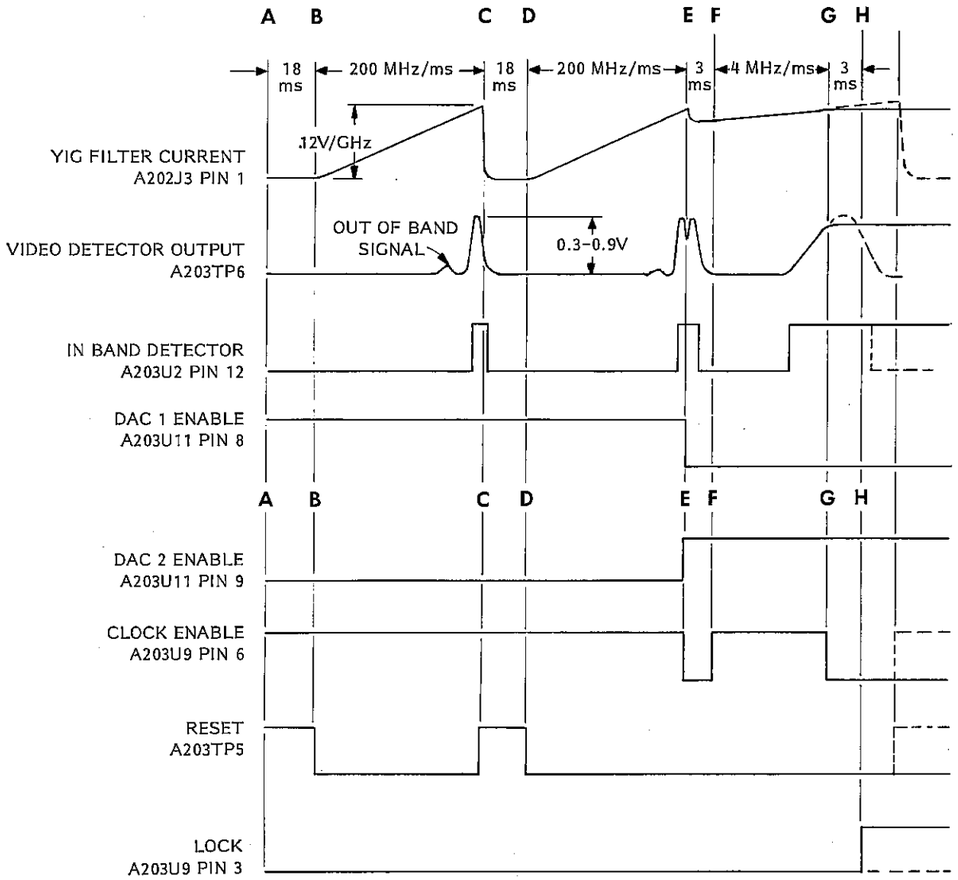
The Peak Detector is discharged by U5B. A CONVERTER RESET command, or lack of the In-Band Detector signal, will activate U5B. The circuit is inhibited from discharging by the presence of the DAC 2 ENABLE command.

The outputs of the two comparators (U2A and U5A), then form input commands to the Signal Acquisition Logic.

Signal Acquisition Logic

There are five commands generated by the Signal Acquisition Logic: CONVERTER RESET, DAC 1 ENABLE, DAC 2 ENABLE, CLOCK ENABLE, and LOCK. The CONVERTER RESET command is an 18 millisecond pulse used to reset the digital logic on both this board and Converter Control 2 (A202), and to enable the Noise Control circuit. The three enable commands determine which DAC (if any) will control the sweep current applied to the YIG filter. If the CLOCK ENABLE is low, no sweep will occur, and the current to the YIG will remain constant. If the CLOCK ENABLE is high, either DAC 1 or DAC 2 (on A202) will generate a current sweep. The appropriate DAC is selected by the DAC ENABLE commands.

FIGURE 9-17A
COMPONENT LOCATOR
CONVERTER CONTROL 1 (A203)



The following description is keyed to the corresponding lettered points on the waveforms shown in Figure 9-17C.

A. Initiation of CONVERTER RESET: A CONVERTER RESET will occur in the digital logic whenever any one of the following occur: (1) CONVERTER RECYCLE command from A104. (2) Either DAC reaching the end of its range. (3) Loss of sufficient video level (U2A input drops below threshold). (4) Image Rejection circuit operating (see later paragraph). When this occurs, U6 pin 1 goes low, causing it to generate an 18 millisecond CONVERTER RESET pulse. This pulse will reset DAC 1, DAC 2, U10B, and U2A.

B. Start Sweep: CONVERTER RESET goes low and enables DAC 1.

C. Presence of Sweep Related Signal: An In-Band signal of sufficient amplitude triggers U2A. When the signal drops below the threshold value, the negative transition triggers flip-flop U10A. This action generates a CONVERTER RESET. All circuits except U10A are reset; U10B is enabled.

D. Start of Second Sweep: End of CONVERTER RESET triggers U10B which, in turn, enables U11A. The purpose of the second sweep is to guarantee that after the signal has been applied to the Converter, a sweep is begun from zero frequency. This prevents locking to a harmonic of the input frequency.

E. Presence of Sweep Related Signal: The negative transition of U2A, as described in paragraph C, triggers U11A. This turns on DAC 2 ENABLE. In addition, multivibrator U6A is triggered, which generates a 3 millisecond pulse. The CLOCK ENABLE is turned off during this pulse, and U7A is triggered. The output of U7A enables U7B. The loss of DAC 1 ENABLE also results in a negative current step (generated on Converter Control 2) such that the YIG/Comb Generator is tuned back through the frequency that initiated the trigger. This action causes the twin peaks in the Video Detector output. During this period, the Peak Detector has stored the peak detected signal level; the voltage at U5 pin 6 is 90% of that peak.

F. Start of DAC 2 Sweep: The CLOCK ENABLE command goes high at the end of the pulse from U6A.

G. Stop Sweep: When the Video Detector output reaches 90% of the stored peak U5A is triggered, which again causes a 3 millisecond pulse to be generated by U6A. This pulse triggers U7B which disables the CLOCK ENABLE.

H. Lock: At the end of the 3 millisecond pulse, the LOCK command is obtained at U9 pin 11 (this allows the counter to display the input frequency). If at any time after LOCK command occurs, the output of the Video Detector should drop below the threshold set at U2 pin 5, a CONVERTER RESET command will be initiated when U2 pin 10 goes high.

Image Rejection

At input levels below the specified sensitivity, it is possible that although the video level is insufficient to trigger U2A on the correct comb line, the next higher line is sufficient. If the counter should lock to this line, called the image, an erroneous reading would result. To prevent this, an image rejection circuit consisting of U11B and U14 is provided.

If the In-Band Detector turns on, then off, without U2A triggering, multivibrator U14B enables flip-flop U11B for 3 milliseconds. If during this period, U2A is triggered, resulting in DAC 1 ENABLE going low, U11B will be triggered, resulting in a CONVERTER RESET. The Converter is thus prevented from locking on the image.

FIGURE 9-17C
OPERATING SEQUENCE
CONVERTER CONTROL 1 (A203)

I. C. NO.	TYPE	PIN NO.				
		GND	+5V	-5.2V	+12V	-12V
U8	DM7400	7	14			
U12	DM7405	7	14			
U9	DM7408	7	14			
U17	DM7420	7	14			
U7, U10, U11	DM7473	11	4			
U6, U14, U18	DM74123	6	1	8		
U16	DM74393	8	16			
U13	CA3049					
U4	CA3130			4	7	
U3	LM741C				7	4
U4	LM7615				7	4
U15	MC1408L-6	1,2	13			3
U2, U5	72506			4	11	

LIMITER

PEAK DETECTOR

LOCK CONTROL

BUFFER

VIDEO DETECTOR

VIDEO THRESH. COMPARATOR

SWEEP CONTROL

RESET GEN.

IN-BAND CIRCUIT

IMAGE REJECTION

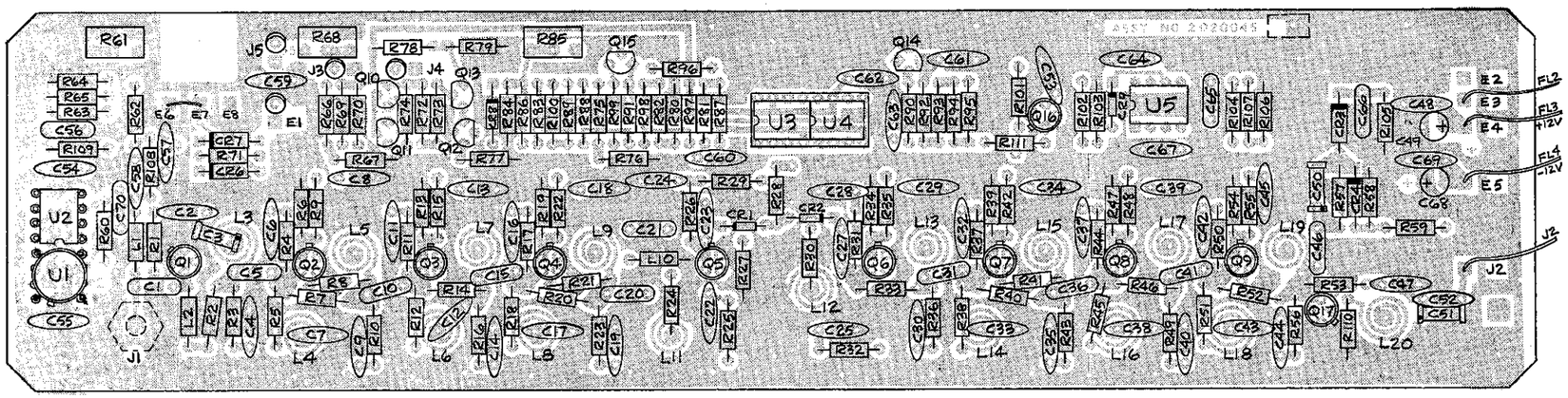
NOISE CONTROL CIRCUIT

△3 PART OF PC BOARD.

△4 MATCHED PAIR.

FIGURE 9-17B
SCHEMATIC DIAGRAM
CONVERTER CONTROL 1 (A203)

066C



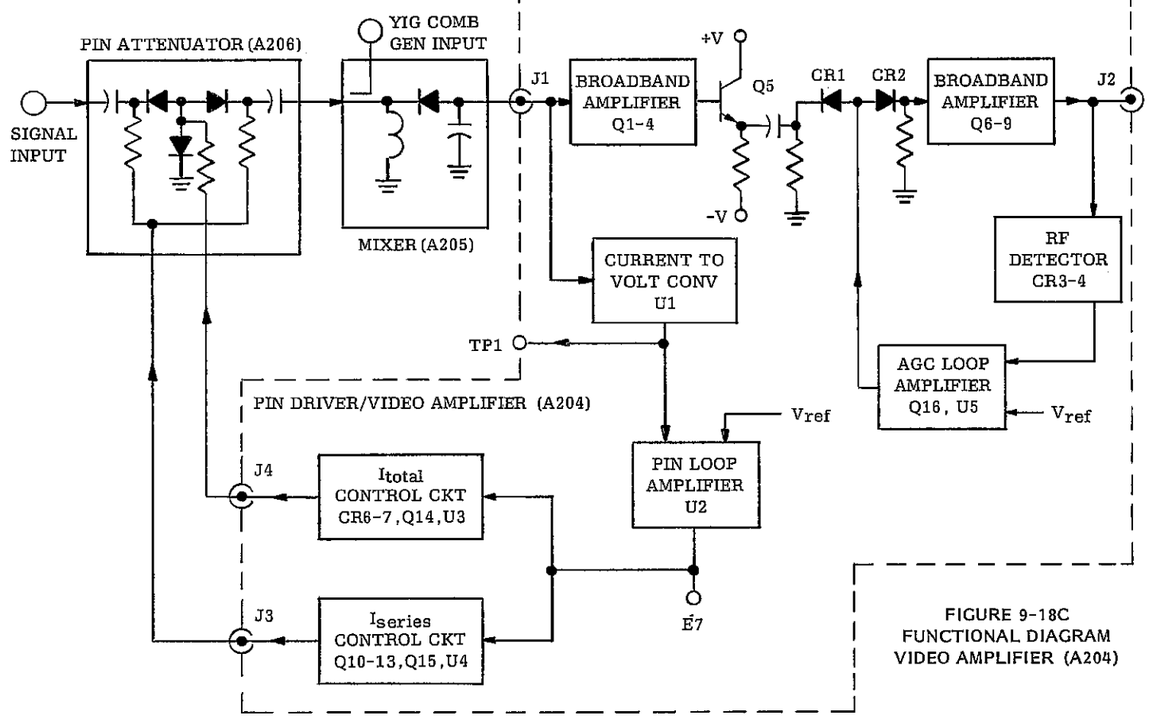


FIGURE 9-18C
FUNCTIONAL DIAGRAM
VIDEO AMPLIFIER (A204)

PIN DRIVER/VIDEO AMPLIFIER (A204)

Refer to Functional Diagram — Figure 9-18C.

The PIN Driver/Video Amplifier module (A204) consists of two distinct sections: the PIN Diode Attenuator Control Loop, and the Video Amplifier.

Components of the PIN Driver include:

a. PIN Diode Attenuator (A206).
b. Mixer (A205).
c. Current-to-Voltage Converter (A204U1).
d. Loop Amplifier (A204U2).
e. I_{series} Control Circuit (A204Q10-13,Q15,U4).
f. I_{total} Control Circuit (A204CR6,CR7, Q14,U3).

Components of the Video Amplifier include:

a. Four-stage Broadband Amplifier (A204Q1-4).
b. PIN Attenuator Section (A204CR1, CR2,Q5).
c. Four-stage Broadband Amplifier (A204Q6-9).
d. RF Detector (A204CR3, CR4).
e. AGC Loop Amplifier (A204Q16,U5).

The PIN Diode Attenuator Control section is a simple feedback loop. DC current from the Mixer diode is converted to a voltage by U1. This voltage is compared to reference voltage (V_{ref}) at the input of U2. The difference in the two voltages is amplified by U2, and appears at E7. This voltage causes the proper currents to flow from the current generators: I_{series} and I_{total}. These currents determine the magnitude of signal attenuation in the PIN Diode Attenuator (A206).

The I_{series} and I_{total} current generators contain shaping networks that control the ratio of the currents through the series and shunt diodes in the attenuator to provide a fairly constant 50 ohm terminal impedance.

The current shaping network for I_{total} consists of CR6, CR7, R68, and R71. CR6 and CR7 produce an approximately exponential curve, while R68 and R71 produce a linear curve. Their sum determines the shape of the current into the summing node at R75.

In operation, an increase in signal power at the attenuator input results in an increase in the magnitude of DC current from the Mixer diode. The increased current causes the outputs from U1 and U2 to tend positive, increasing I_{total} while decreasing I_{series}. This produces an increase in the current through the shunt diode, and a decrease in the current through the series diodes, in a ratio which maintains a 50 ohm terminal impedance. This action decreases the magnitude of change in signal power which appears at the Mixer diode.

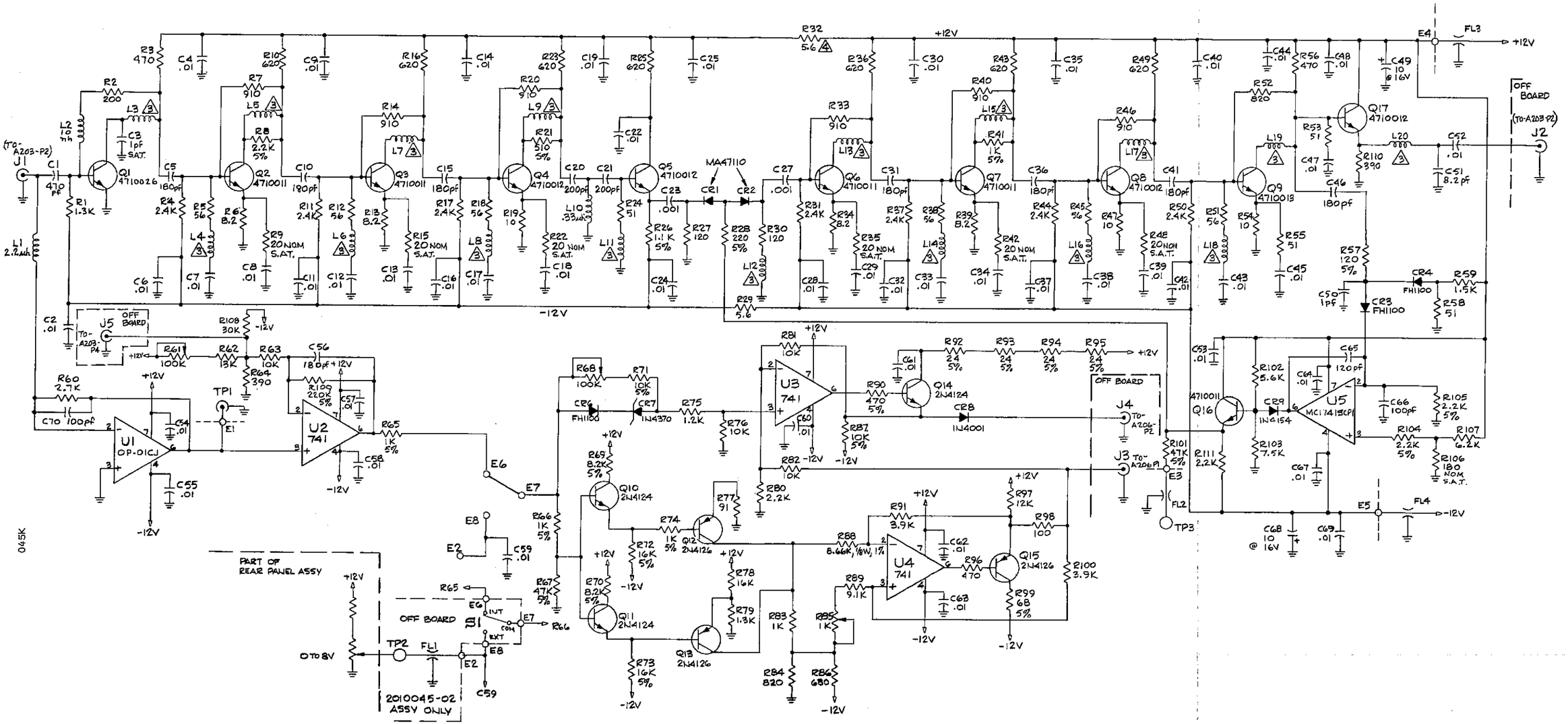
The Video Amplifier section amplifies the difference frequency produced by the Mixer, and applies it to Converter Control 1 (A203).

The circuit consists of eight essentially identical gain blocks and an automatic gain control. Overall gain of the Video Amplifier is nominally 56 dB, with a frequency range of 25 MHz to 275 MHz.

A typical gain block includes a single broadband transistor amplifier stabilized by series and shunt feedback, and an output matching inductor.

The AGC portion of the amplifier consists of RF level detector CR3 and CR4, loop amplifier U5, PIN Diode current driver Q16, emitter follower Q5, and PIN Attenuator diodes CR1 and CR2. The reference voltage in the AGC loop sets the maximum output power level for the Video Amplifier at 0 to +1 dBm.

FIGURE 9-18A
COMPONENT LOCATOR
VIDEO AMPLIFIER (A204)



3 PART OF PC BOARD.

FIGURE 9-18B
SCHEMATIC DIAGRAM
VIDEO AMPLIFIER (A204)

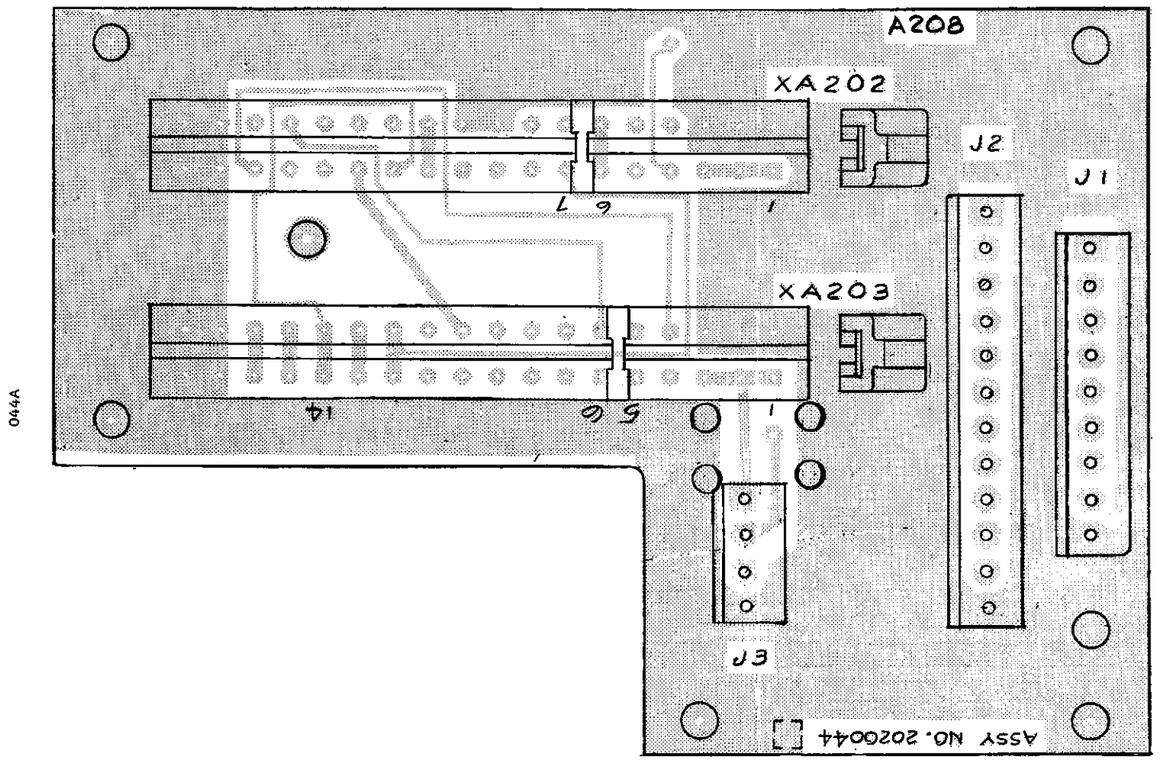


FIGURE 9-19A
COMPONENT LOCATOR
CONVERTER INTERCONNECT (A208)

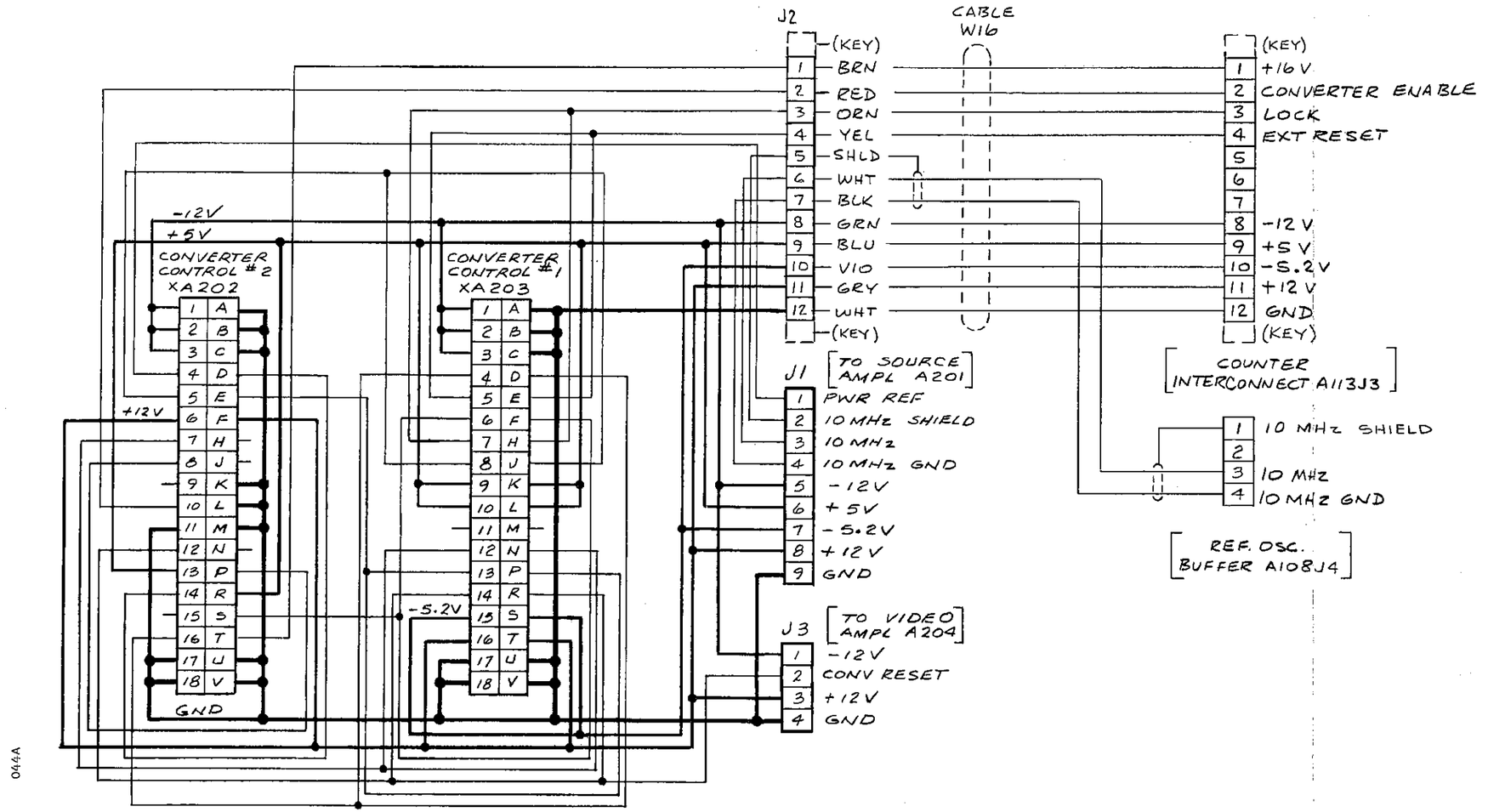
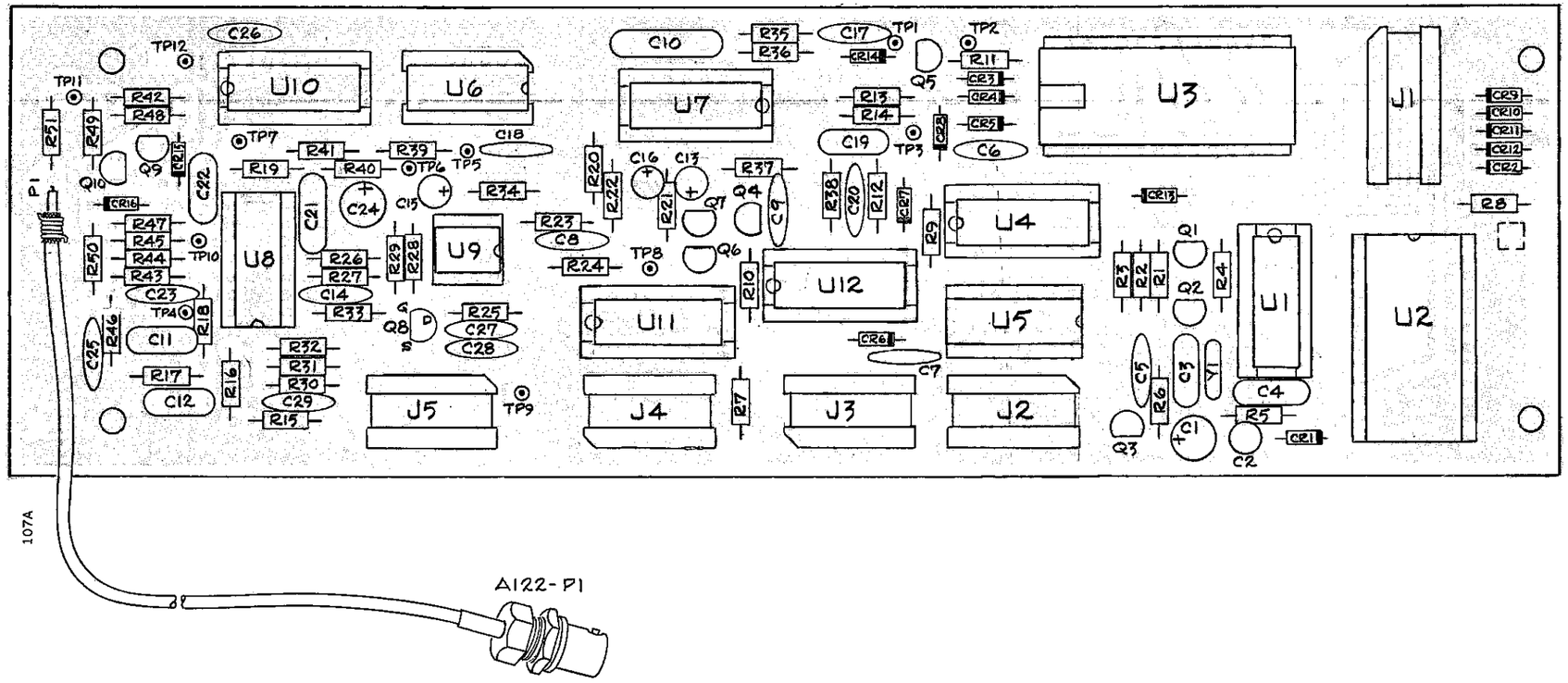


FIGURE 9-19B
SCHEMATIC DIAGRAM
CONVERTER INTERCONNECT (A208)



MICROPROCESSOR (A122)

A122 contains the microprocessor (μP) which controls all of the data manipulation and mathematical computation to perform the YIG Preset, Phase Lock, and Band Change functions.

The heart of the μP board is the 4040 Microprocessor (U2). U2 requires two clock signals and a Power On Reset signal which are supplied by clock generator U1. All the signals for data to and from the μP, are carried on the 1-bit Test input, the 1-bit Carry output line, or the 4-bit bi-directional data lines (D_0 - D_3).

The 4-bit data lines are connected between U2 and U3. U3 is a combination ROM (read only memory), and I/O (input/-output) IC. The ROM contains the program steps that control the programming of U2. The four I/O ports are 4-bits each, resulting in 16 data I/O lines. These lines are set up as four input lines, and twelve output lines. These 16 lines, plus the Test input and Carry output on U2, control all the data manipulation in the system.

Data Input

Data input to the μP follows one of two basic methods: Serial data input, or parallel data input. Parallel input is the simplest method, but it requires one input port for each data bit. It is, therefore, used in only one place in the system: the input from the keyboard (KEY 0 - KEY 2).

The remainder of the input data is read by a serial input data process. Two 8-bit shift registers (U11, U12), are used to input appropriate data. The process begins with a series of commands which load U11 and U12 with the 16 bits of data on their inputs. After the Load command, the first piece of data (Converter Lock) is available on the Test input to U2. For each subsequent piece of data, a clock pulse shifts register data up one bit. To read any piece of data requires N-1 clock pulses, where N equals the number of bits down on the shift register where the data is located.

Data Output

Data output also occurs in both serial and parallel modes. The parallel mode is used only for the 4-bit BCD number which lights the numerical display (MUX A - MUX D). All other data is sent out in the serial mode. In this mode, the data is presented one bit at a time, on the Carry Output of U2. While the data is present, a clock pulse is sent to clock the data into an appropriate shift register. For the serial output routine, one clock pulse is required for each bit of data to be read out. Data which is to be sent out by this process includes YIG Preset, PLL Program, Gain Adjust, and Band Select.

Loop Amplifier

The Loop Amplifier has essentially three stages of gain (U8A, B, and C). U8A is a 2-pole low pass filter. It has a DC gain of two, and a corner frequency of 16 kHz. Above the corner frequency, the gain drops off at the rate of 12 dB per octave.

U8B is a summing amplifier used to combine the signal from the oscillator (U7) with the video from U8A, and also with an external input (TP6) for introducing signals for loop test purposes. U8C, in combination with U10, is a digitally controlled gain stage. U10 is designed to be used with a summing amplifier and an internal 10 K ohm feedback resistor, to give a gain that is proportional to the binary number programmed. (The gain of this stage would normally be .0078 to .999 using the internal 10 K feedback resistor. However, resistor R42 has been added to increase the gain by a factor of 1.3, resulting in a .01 to 1.3 gain range.) The gain of U10 is programmed by the μP through U6. The program is written such that the gain can be stepped in approximately 3 dB steps.

Bandwidth Adjust Oscillator

U7 is a dual frequency monolithic waveform generator. The frequency of the oscillator is determined by the Select line (FSK) on U7 pin 9. When pin 9 is low, the frequency is determined by C10/R14. When pin 9 is high, the frequency is determined by C10/R13. A sine wave is obtained by first generating a triangular wave, then driving a triangle-to-sine wave converter. The purity of the resulting waveform is a function of how hard the converter is driven. R37 controls the drive to the converter, with its value selected for best signal purity.

Bandwidth Detector

The bandwidth detector (Q8-8, U8D, U9A/B), consists of three circuits: a DC restorer, a synchronous detector, and a Schmitt trigger. The DC restorer (U8D) functions by having a simultaneous DC gain of +10 and -10. This results in an output level close to zero volts for any DC input. The positive gain however, is bypassed for high frequencies, with the resulting gain for AC signals being -10. This stage drives synchronous detector U8A/B.

The synchronous detector functions by changing the gain of an amplifier from +1 to -1 in accordance with the polarity of the signal to be detected — that is, the gain is +1 when the signal is positive, and -1 when the signal is negative. The detector output essentially resembles that of a full wave rectifier. The amplifier output is passed through an integrator (R24/C13), whose output is a DC voltage proportional to the amplitude of the incoming signal. All signals not synchronous with the switching rate of the amplifier, have equal positive and negative gains, resulting in an average DC value of zero volts. The output of the synchronous detector drives a Schmitt trigger (Q6, Q7), which has about 250 mV of hysteresis. The output switches to a high at an input threshold of 1.33 volts, and to a low at an input threshold of 1.08 volts.

The automatic bandwidth adjustment process begins with the loop at its lowest gain (narrowest bandwidth). Oscillator U7 is turned on, with its output driving U8B; the output from U8B drives the synchronous detector. At narrow bandwidths, the peak detector sees the signal and sends out a high, indicating that the bandwidth is too narrow. The automatic programming increases the gain of the loop by stepping U10 in 3 dB increments. As the bandwidth increases, the frequency generated by U7 becomes a frequency inside the loop bandwidth. When this happens, the loop feeds back some signal at the output of U8A which is out of phase with that from U7. This feedback cancels some of the signal from the oscillator, and at the appropriate bandwidth, the output of U8B is small enough that the synchronous detector output goes low, indicating sufficient bandwidth.

FIGURE 9-20A
COMPONENT LOCATOR
MICROPROCESSOR (A122)

I.C. NO.	TYPE	PIN NO. GND	+5V	+12V	-12V	-10V	H/C
U1	4201		15			4	
U2	4040		9			14	
U3	4308		1			28	
U4	CD4010AE	8	1,16				13
U5, U6	74LS164	7	14				
U7	XR2206	12		4			
U8	UA4136			11	7		
U9	MC1458			8	4		
U10	AD7530	3		14			
U11,U12	CD4014AE	8	16				

* INDICATES 2% TOLERANCE.

ALL DIODES ARE EIP P/N: 2704154.

FIGURE 9-20B
SCHEMATIC DIAGRAM
MICROPROCESSOR (A122)

107A

AUXILIARY DISPLAY (A123)

The Auxiliary Display board (A123) has three functions: to display the data entry digits for YIG Preset, and Phase Lock frequency; to light the BAND SELECT, PRESET, and LOCK status indicators; and to scan the keyboard for data entry. All signals to and from A123 are fed through J1, with the exception of local Band Select (on P1).

The keyboard display scan consists of a set of clock and data pulse pairs generated by the microprocessor on A122. The clock and data signals enter via J1, and drive U3 pins 8 and 2 respectively. Each scan sequence consists of eight clock pulses, with the data input being low for the first pulse, and high for all other pulses. The data low is shifted down the shift register from Q(A) to Q(H), sequentially enabling eight components of display. The first step, which enables either the YIG PRESET or LOCK indicator, is about three times longer than that for the remaining display digits, to equalize the apparent brightness of the different types of displays.

Each display digit is lit by the MUX A through MUX D information. The MUX data is changed from a blank display character to the desired display character shortly after the enable is turned on, and changed back to a blank character shortly before shifting the enable to the next desired character. For those digits which are to be blanked, the blank character is simply left on the MUX line during the enable time.

The keyboard data entry is examined at each of the enable times. Since all three key lines have pull up resistors internal to the ROM input port, they are all high unless a key is pressed. When a key is pressed, the low level from the scan shift register (U3) is connected through the keyboard to one of the key lines. The status of U3 is compared to the key line input data, and the selected key is decoded. If two or more keys are pressed simultaneously, the keyboard data is decoded as invalid, and is ignored.

Band select data is sent out each time the BAND SELECT key is pressed. The local band select is programmed by four clock and four data pulses. The band select data is is negative logic data — that is, a low on the appropriate band select line lights the BAND SELECT indicator, and selects the local band. Since a remote band selection could be different than a local band selection, the band select data is sent out twice each time the band is changed. Local band data is sent out, then the existing band select data is read and sent out. If the counter is in the local mode, the two band selects will be the same. If the counter is in the Remote mode, the second band select data will match the remote band selected.

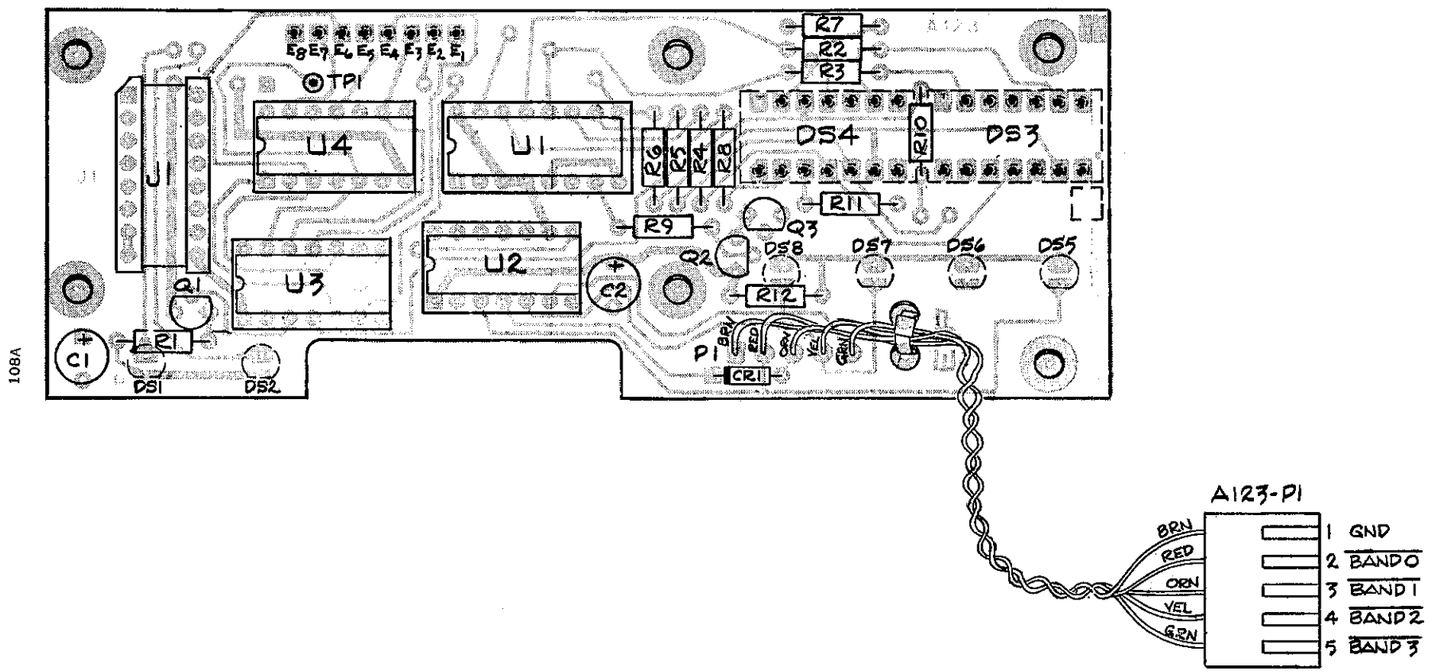
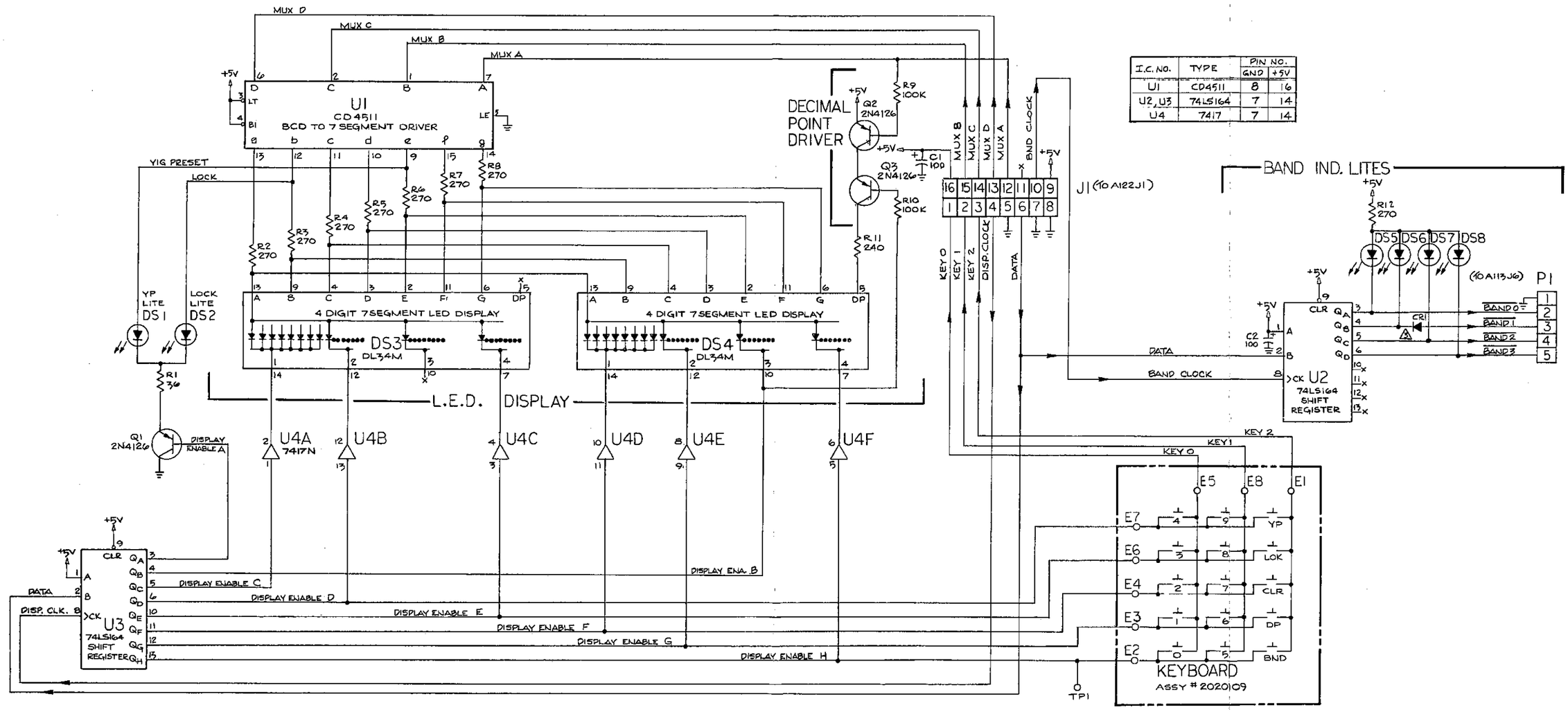


FIGURE 9-21A
COMPONENT LOCATOR
AUXILIARY DISPLAY (A123)

I.C. NO.	TYPE	PIN NO.	
		GND	+5V
U1	CD4511	8	16
U2, U3	74LS164	7	14
U4	7417	7	14



108A

3 EIP P/N: 2710016.

FIGURE 9-21B
SCHEMATIC DIAGRAM
AUXILIARY DISPLAY (A123)

SECTION O

OPTIONS

O-1. This section provides descriptions, specifications (where applicable), schematic diagrams and component locators, for the options available for use with the EIP 371 Source Locking Microwave Counter.

OPT	DESCRIPTION
03	OVEN STABILIZED OSCILLATOR (5×10^{-9})
04	OVEN STABILIZED OSCILLATOR (1×10^{-9})
05	OVEN STABILIZED OSCILLATOR (5×10^{-10})
06	PROGRAMMABLE OFFSETS
07	REMOTE PROGRAMMING
09	BCD OUTPUT
10	REAR PANEL INPUT CONNECTORS
11	BAND II DELETED
13	RACK MOUNT/CHASSIS SLIDES
17	GENERAL PURPOSE INTERFACE BUS*

* See separate manual

NOTE: Options 01, 02, and 12 are not used with the 371 Source Locking Counter.

OPTION 01
YIG PRESET - PROGRAMMABLE

O1-1. DESCRIPTION

O1-2. This option allows the user to program the starting frequency of the sweep in Band III (825 MHz to 12.4/18 GHz). Increments of 200 MHz may be programmed by grounding the appropriate inputs using standard 1-2-4-8 BCD code. These inputs drive Converter Control 2 inverters A202U7 and U9 to preset the DCUs of DAC 1 on A202.

O1-3. For proper Converter operation, it is necessary that the sweep function not be interfered with. This requires that the minimum frequency to be measured must be at least 275 MHz above the preset frequency. It also imposes the requirement that the preset number be at least 275 MHz above any other frequencies present.

O1-4. Provided the above restrictions are met, Option 01 may be used both for the purpose of speeding acquisition time, and to measure a signal in the presence of a lower frequency signal.

J3 Pin No.	Function
16	10^8 B (200 MHz)
17	10^8 C (400 MHz)
18	10^8 D (800 MHz)
19	10^9 A (1 GHz)
20	10^9 B (2 GHz)
21	10^9 C (4 GHz)
22	10^9 D (8 GHz)
23	10^{10} A (10 GHz)
24	Ground
25	+ 5 Vdc

TABLE O1-1
J3 CONTACT GROUNDING FOR PROGRAMMABLE YIG PRESET OPTION 01

O1-5. OPERATION

a. Enter preset frequency into the counter with consideration for programming requirements.

b. Press RESET button.

EXAMPLE: To measure 8 GHz signal in presence of 4 GHz signal (both signals above minimum sensitivity of counter), program counter for 7 GHz; press RESET button. Counter begins sweep at 7 GHz and locks on 8 GHz signal.

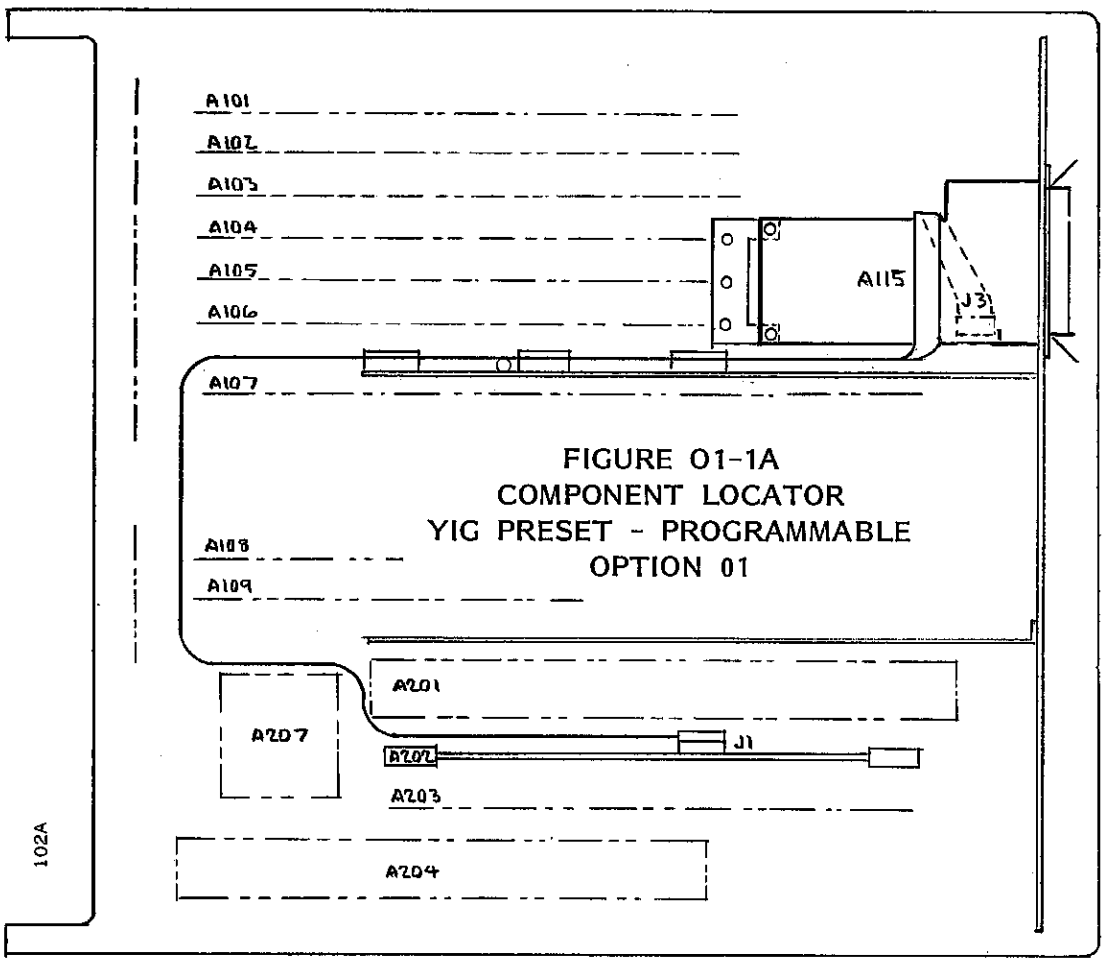
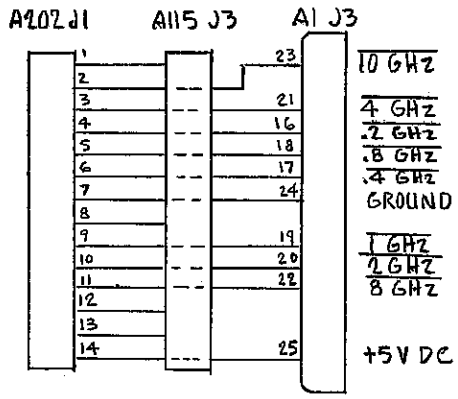


FIGURE 01-1A
COMPONENT LOCATOR
YIG PRESET - PROGRAMMABLE
OPTION 01



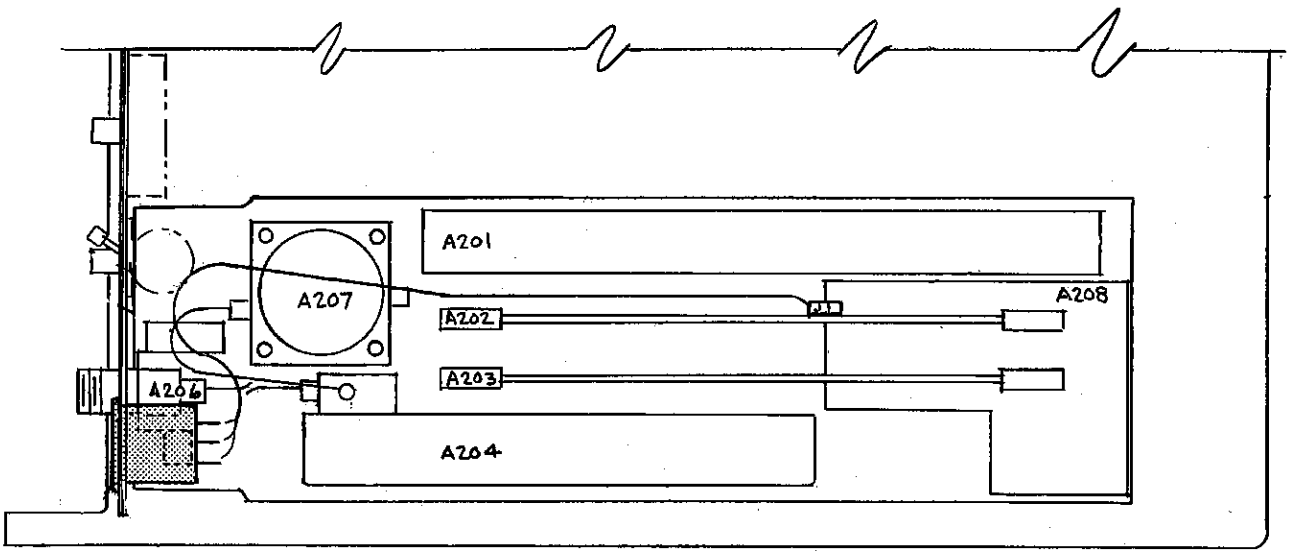
Refer to Option 07, Figure 07-1 for Component Locator and Schematic Diagram for A115 Programming board.

FIGURE 01-1B
INTERCONNECTION DIAGRAM
YIG PRESET - PROGRAMMABLE
OPTION 01

OPTION 02
YIG PRESET - THUMBWHEEL

02-1. DESCRIPTION

02-2. This option is functionally identical to Option 01 with the exception that ground contact closure is provided by a 3-digit thumbwheel switch mounted on the front panel of the counter. Comb start frequency may be read directly from the switch.



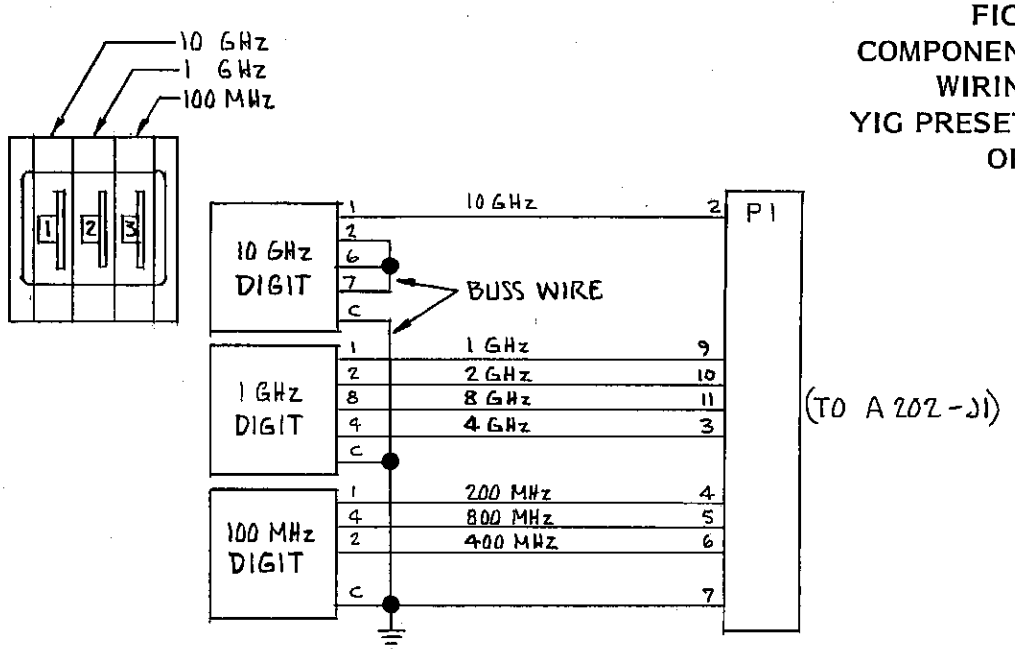


FIGURE 02-1
COMPONENT LOCATOR AND
WIRING DIAGRAM
YIG PRESET - THUMBWHEEL
OPTION 02

OPTIONS 03, 04, AND 05
HIGH STABILITY TIME BASE
(OVEN STABILIZED CRYSTAL OSCILLATOR)

O3-1. DESCRIPTION

O3-2. Three Oven Stabilized Oscillators are available as options for certain EIP Autohet Counters. Specifications for the three options are listed in Table O3-1. These options reduce the counter inaccuracy (see Section 6) due to both temperature and time.

O3-3. When either Option 03, 04, or 05 is installed, the TCXO (A116) is removed from the Reference Oscillator PC Board (A108), and components are added to A108 and Counter Chassis A1 (see Section 9, Figure 9-10). The added components include Oven Oscillator power transformer A114T1, 28 Vdc Oven Power Supply A114, and connector A108J3.

O3-4. The 28 volt Power Supply is on and operating as long as the counter is plugged into an active source of AC power, irrespective of the counter's POWER On/Off switch. Primary wiring of the oven oscillator power transformer is shown in Section 9, Figure 9-9. The balance of the circuit is conventional: full-wave bridge rectifier CR1, filter C1, regulator U1, series pass transistor Q1, protective diodes CR1-CR3, and voltage control R3.

CHARACTERISTIC	OPTION 03	OPTION 04	OPTION 05
AGING RATE/24 HOURS (After 72 hour warm-up)	$< \lvert 5 \times 10^{-9} \rvert$	$< \lvert 1 \times 10^{-9} \rvert$	$< \lvert 5 \times 10^{-10} \rvert$
SHORT TERM STABILITY (1 second average)	$< 1 \times 10^{-10}$ rms		
0° to +50° C TEMPERATURE STABILITY	$< \lvert 6 \times 10^{-8} \rvert$	$< \lvert 3 \times 10^{-8} \rvert$	$< \lvert 3 \times 10^{-8} \rvert$
±10% LINE VOLTAGE CHANGE	$< \lvert 5 \times 10^{-10} \rvert$	$< \lvert 2 \times 10^{-10} \rvert$	$< \lvert 2 \times 10^{-10} \rvert$

TABLE O3-1
SPECIFICATIONS
OVENIZED OSCILLATOR OPTIONS

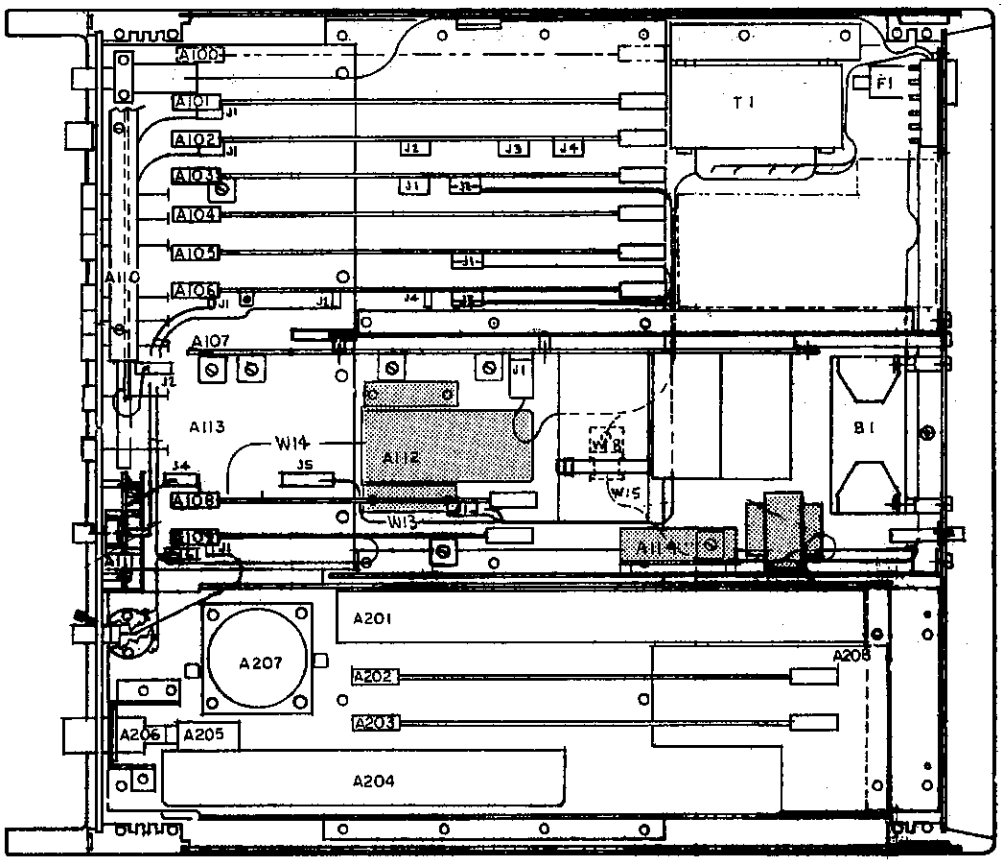
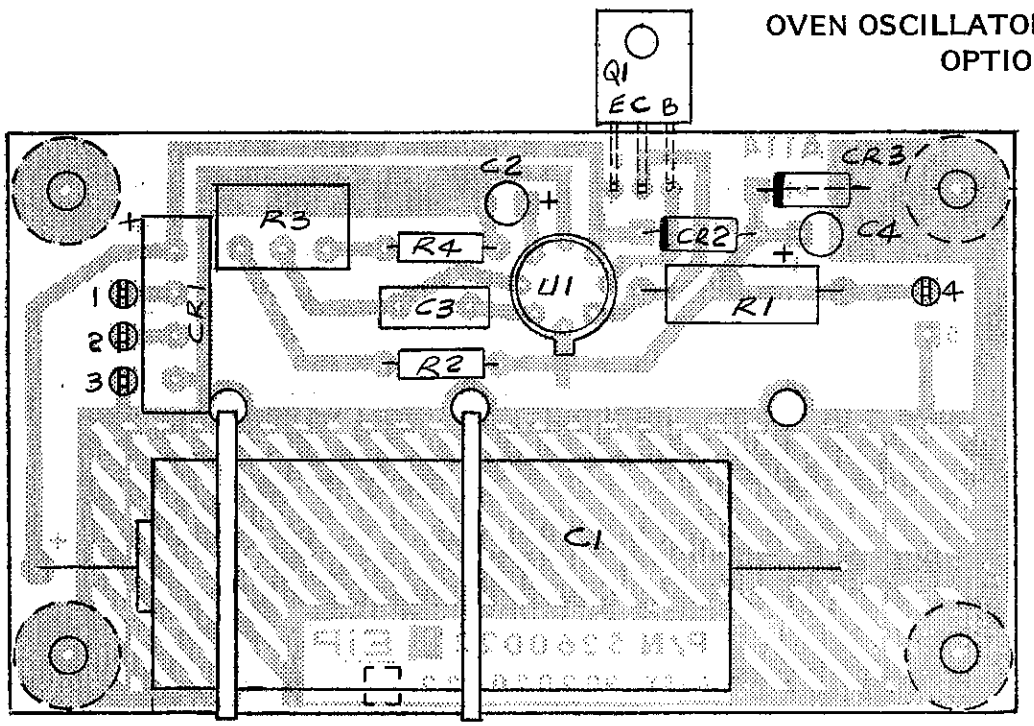


FIGURE 03-1A
COMPONENT LOCATORS
OVEN OSCILLATOR POWER SUPPLY
OPTIONS 03, 04, 05



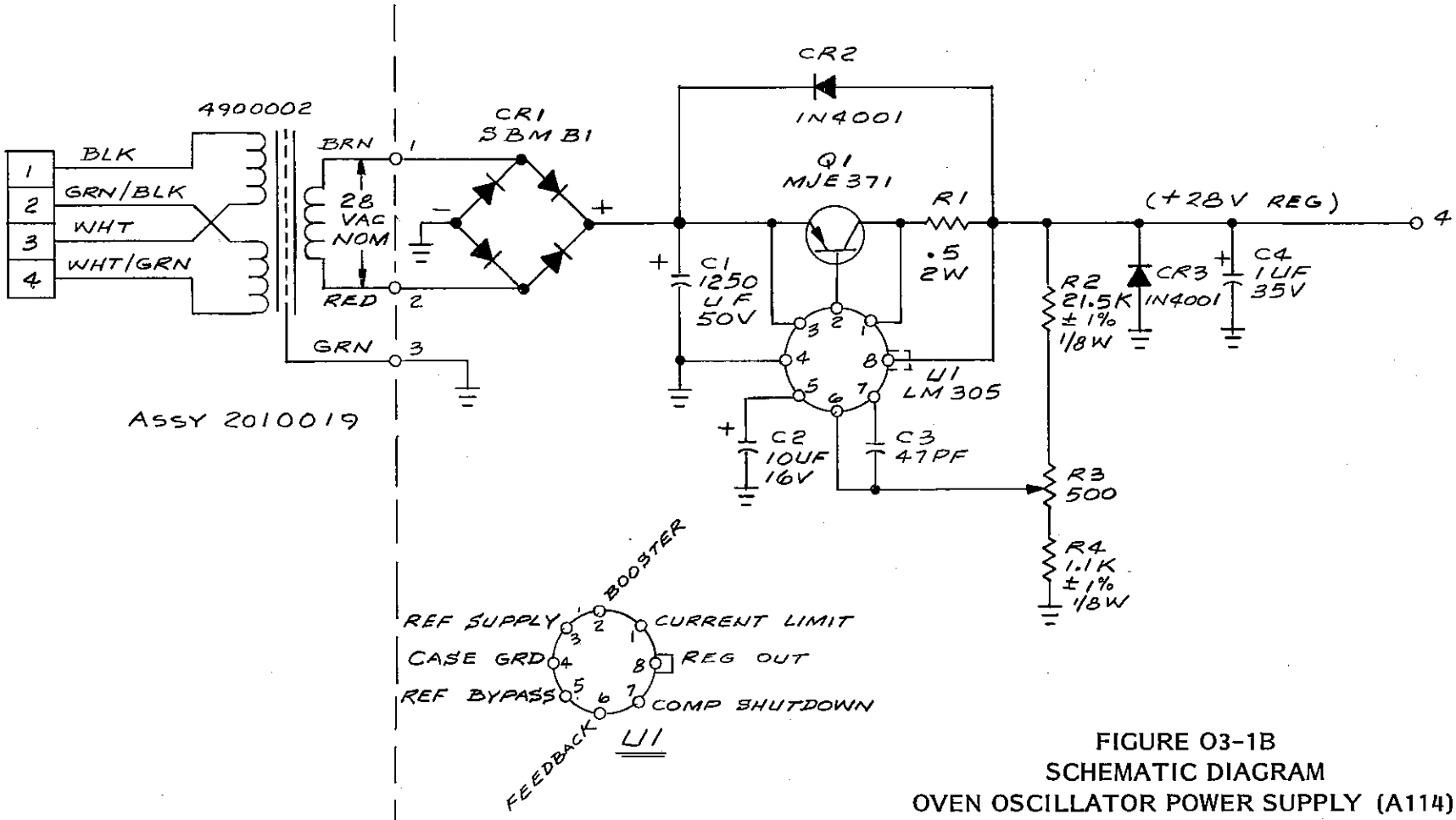


FIGURE 03-1B
SCHEMATIC DIAGRAM
OVEN OSCILLATOR POWER SUPPLY (A114)
OPTIONS 03, 04, 05

OPTION 06
PROGRAMMABLE OFFSETS

O6-1. GENERAL DESCRIPTION

O6-2. This option allows the displayed reading of any frequency to be increased or decreased by any number in 100 kHz increments.

O6-3. For positive offsets, the desired number may be programmed directly on 24 input lines (4-line BCD code on each of six digits). Activating the $\overline{\text{OFFSET ENABLE}}$ command will then cause the reading to be offset by the programmed frequency.

O6-4. Negative offsets require that the nines complement of the number be programmed and that the $\overline{\text{OFFSET MINUS}}$ command be activated. The nines complement of a number is obtained by subtracting the number from 99.9999 GHz.

O6-5. All inputs are programmed by ground contact closure or application of a TTL "0" level. Pin connections are shown in Table O6-1.

O6-6. CIRCUIT DESCRIPTION

O6-7. Circuitry required for the option is contained on two PC boards. Programming Option Board A115 contains the inverters used as buffers for the input information. Offset Control Unit A100 contains the remaining control circuitry.

O6-8. The six digit offset input is used to directly preset the six DCUs on Count Chain 2 (A102). This then requires that the 3 MSD information from the Converter (in Band III operation) must be serially added to the preset information. This is the major function of the Offset Control unit.

O6-9. The second function of the unit is to provide a single pulse to the 100 kHz DCU of A102 during negative offset.

O6-10. During $\overline{\text{SEQUENCE GENERATOR "0"}}$, 3 MSD information from the Converter is preset into U6, U7, and U8. The $\overline{\text{OFFSET LOAD}}$ command is generated (U2 pin 6) and, if $\overline{\text{OFFSET MINUS}}$ is low (negative offset), U4B is set.

O6-11. At $\overline{\text{SEQUENCE GENERATOR "1"}}$, U3A is enabled and divides the input 2.5 MHz clock to 1.25 MHz. U3B inhibits the sequence generator and enables U4A. The first clock pulse triggers U4A which activates the GATE X 100 MHz signal and operates a single ADD X 100 kHz pulse if negative offset is selected. Clock pulses then simultaneously appear at the ADD X 100 MHz output and the $\overline{\text{COUNT DOWN}}$ input to U6. Pulses continue until U6, U7, and U8 have counted down to zero. U3B is then reset, which in turn resets U4A, ends the cycle, and removes the $\overline{\text{SEQUENCE GENERATOR INHIBIT}}$.

O6-12. Programming connector type: Amphenol 57-40500, 50 pin female. Mating connector: Amphenol 57-30500, 50 pin male.

J3 Pin	Function
14	Ground
15	Offset $\overline{\text{Enable}}$
26	10^5 A (100 kHz)
27	10^5 B (200 kHz)
28	10^5 C (400 kHz)
29	10^5 D (800 kHz)
30	10^6 A (1 MHz)
31	10^6 B (2 MHz)
32	10^6 C (4 MHz)
33	10^6 D (8 MHz)
34	10^7 A (10 MHz)
35	10^7 B (20 MHz)
36	10^7 C (40 MHz)
37	10^7 D (80 MHz)
38	10^8 A (100 MHz)
39	10^8 B (200 MHz)
40	10^8 C (400 MHz)
41	10^8 D (800 MHz)
42	10^9 A (1 GHz)
43	10^9 B (2 GHz)
44	10^9 C (4 GHz)
45	10^9 D (8 GHz)
46	10^{10} A (10 GHz)
47	10^{10} B (20 GHz)
48	10^{10} C (40 GHz)
49	10^{10} D (80 GHz)
50	Offset Plus/$\overline{\text{Minus}}$

TABLE O6-1
J3 CONTACT GROUNDING FOR
PROGRAMMABLE OFFSET
OPTION 06

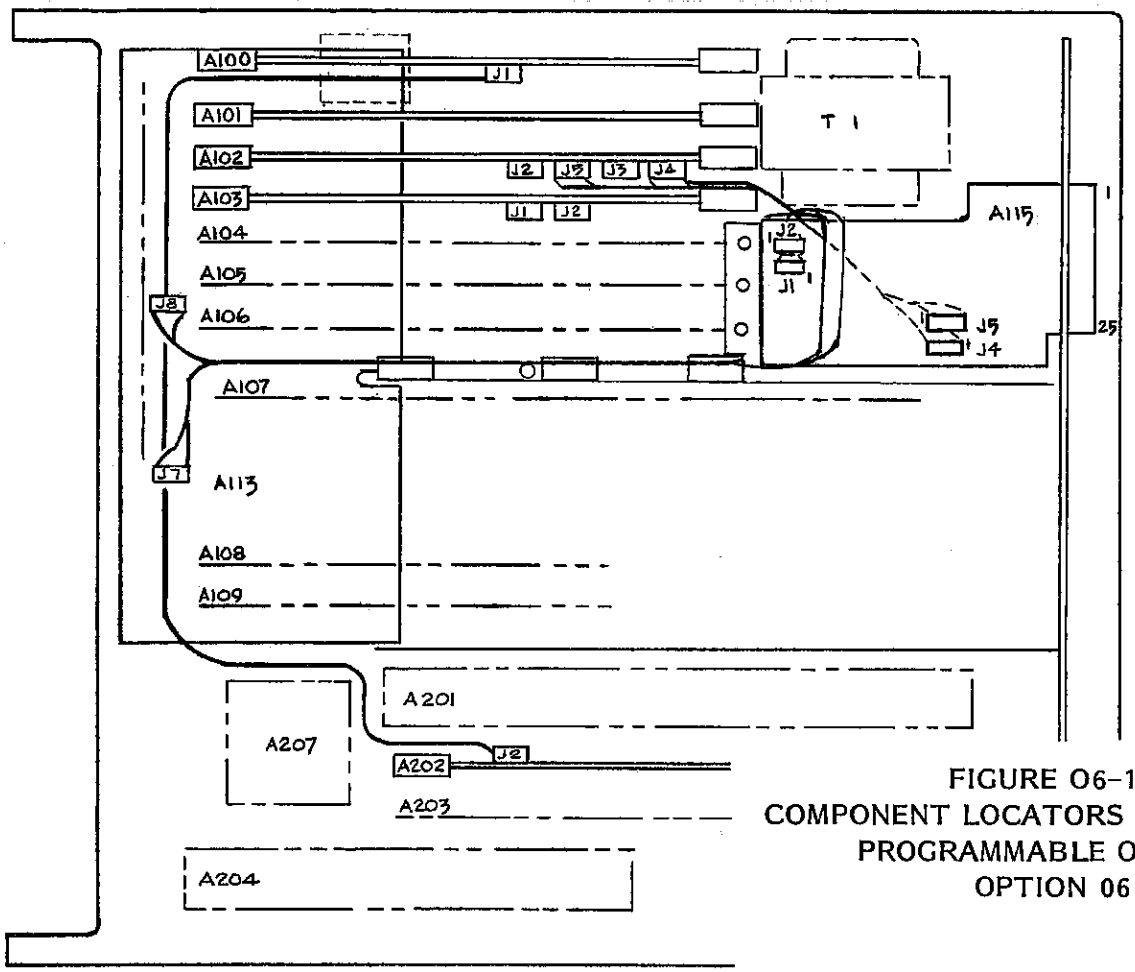
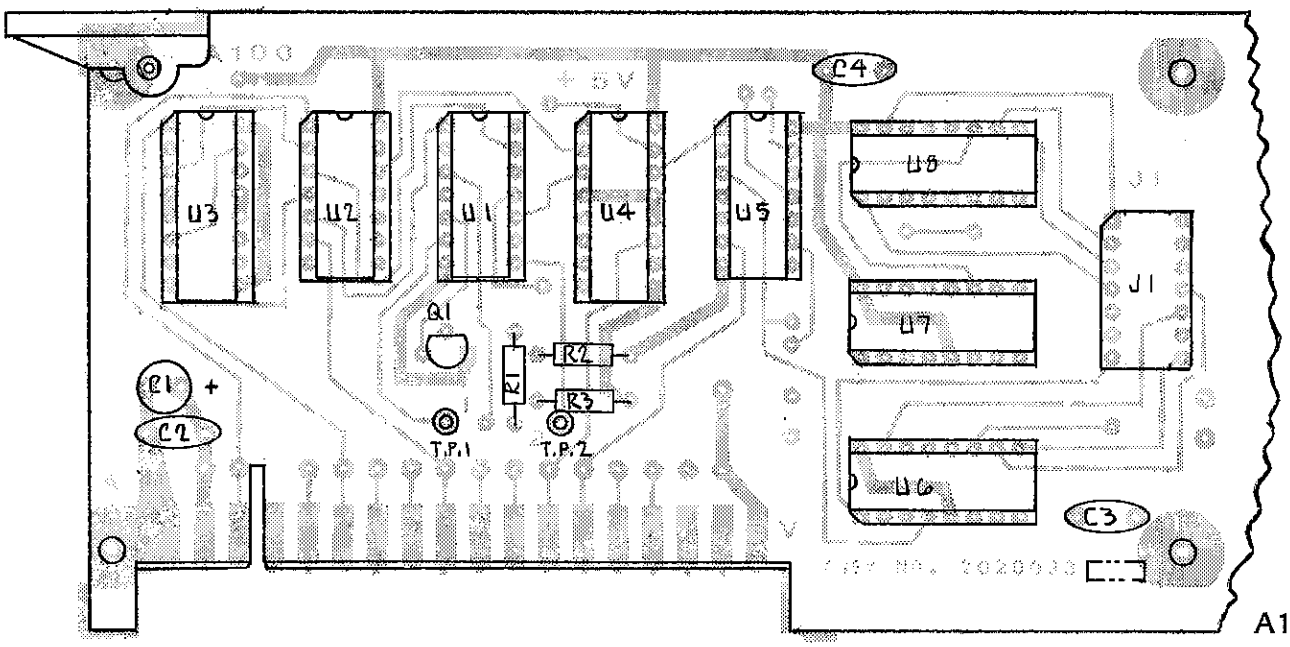


FIGURE O6-1A
COMPONENT LOCATORS (A100 & A115)
PROGRAMMABLE OFFSETS
OPTION 06

Refer to Option 07, Figure O7-1 for Component Locator and Schematic Diagram for A115 Programming Board.



A100

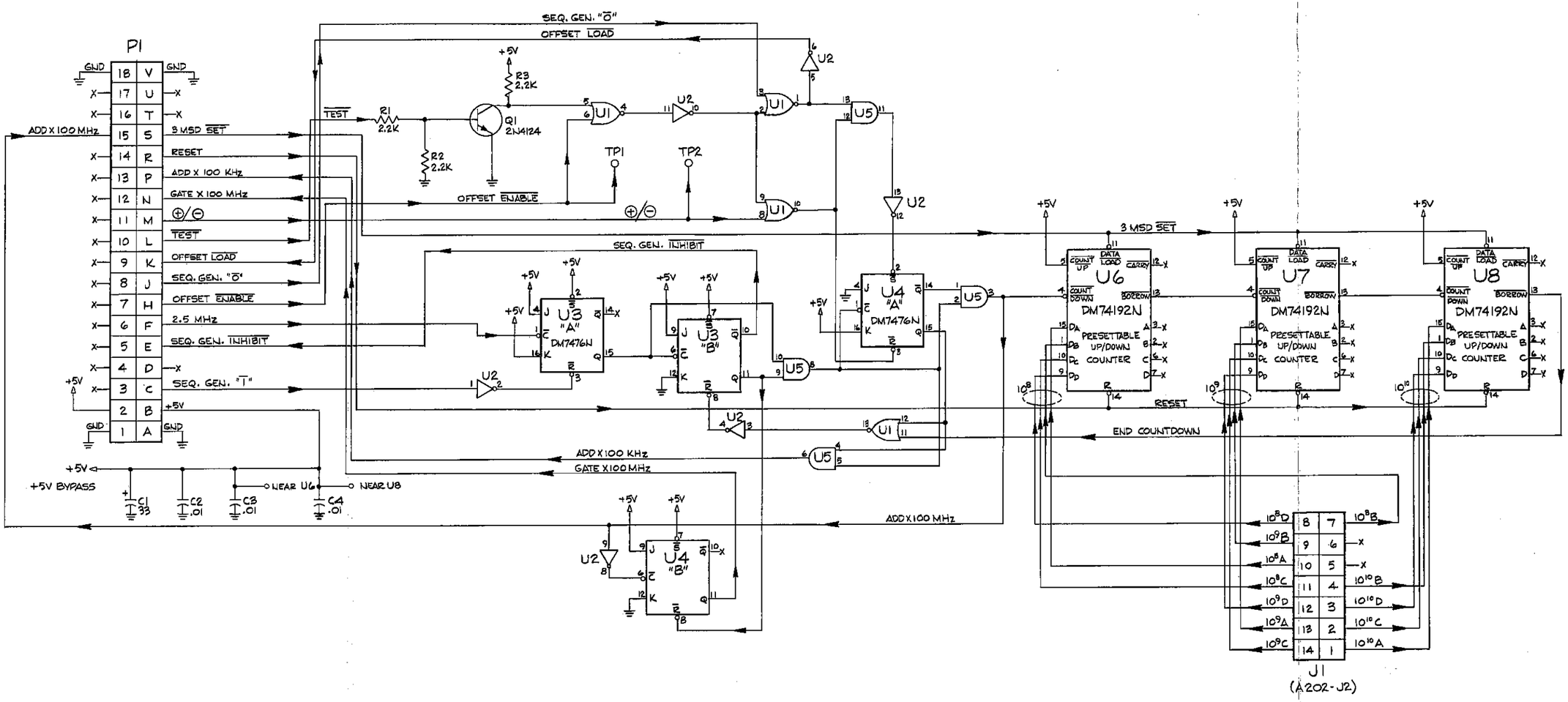


FIGURE 06-1B
SCHEMATIC DIAGRAM
PROGRAMMABLE OFFSETS
OPTION 06

OPTION 07
REMOTE PROGRAMMING

O7-1. GENERAL DESCRIPTION

O7-2. Most of the functions which are normally controlled from the front panel of the counter may be remotely programmed by this option. These functions are:

a. 10 Hz RESOLUTION
b. 100 Hz RESOLUTION
c. 1 kHz RESOLUTION
d. HOLD
e. RESET
f. TEST
g. BAND I SELECT
h. BAND II SELECT
i. BAND III SELECT

O7-3. In addition to the front panel controls, an additional command: COUNTER RESET is also available. This command resets the counter and initiates a new reading without resetting the Converter.

O7-4. The LOCAL/$\overline{\text{REMOTE}}$ input activates the remote functions. This and all remote commands are activated by ground contact closure or a TTL "0" level. Pin connections to the rear panel are shown in Table O7-1.

O7-5. CIRCUIT DESCRIPTION

O7-6. In the standard instrument, all front panel control switches are returned to ground through a jumper cable between A113J7 and J8. With Option 07, the jumper cable is removed, and cables from J7 and J8 connect to Remote Programming board A115. Switch returns are grounded through circuits on A115 in the LOCAL mode. In $\overline{\text{REMOTE}}$, a series of multiplexers disable the front panel switches and enable the remote control lines.

O7-7. The remote programming circuit contains 13 two-input multiplexers, each of which has one input connected to a front panel switch return, and one input connected to the REMOTE PROGRAMMING connector. When the LOCAL/$\overline{\text{REMOTE}}$ line (J3 pin 13) is grounded, the multiplexers effectively open the ground connections of the front panel controls, allowing remote control of functions shown in Table O7-1.

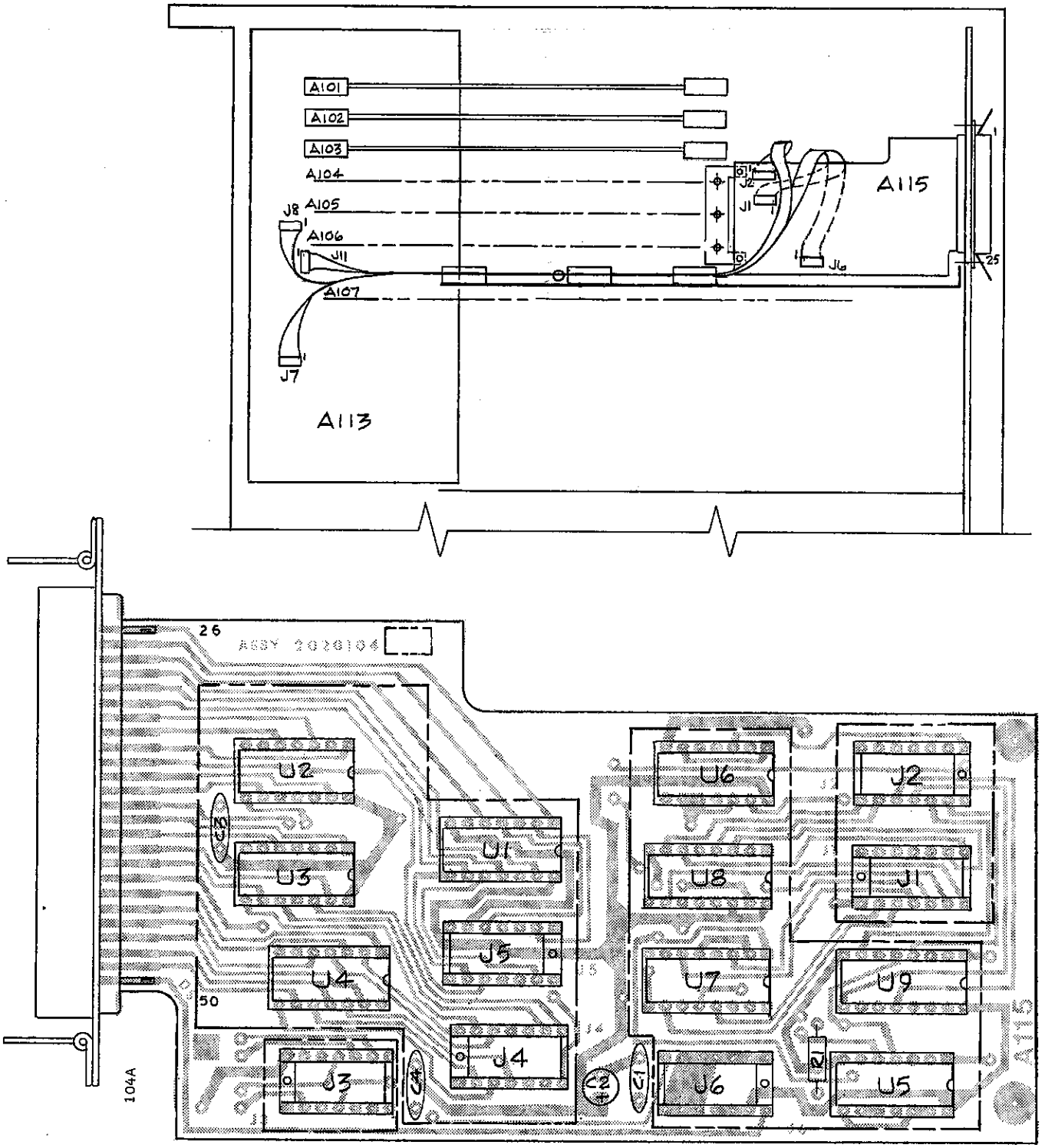
O7-8. If the $\overline{\text{HOLD}}$ is not energized, front panel SAMPLE RATE determines cycle time. In remote operation, front panel HOLD is ineffective.

O7-9. If none of the RESOLUTION switches are grounded, the counter will operate with a one second gate.

O7-10. Programming connector type: Amphenol 57-40500, 50 pin female. Mating connector: Amphenol 57-30500, 50 pin male.

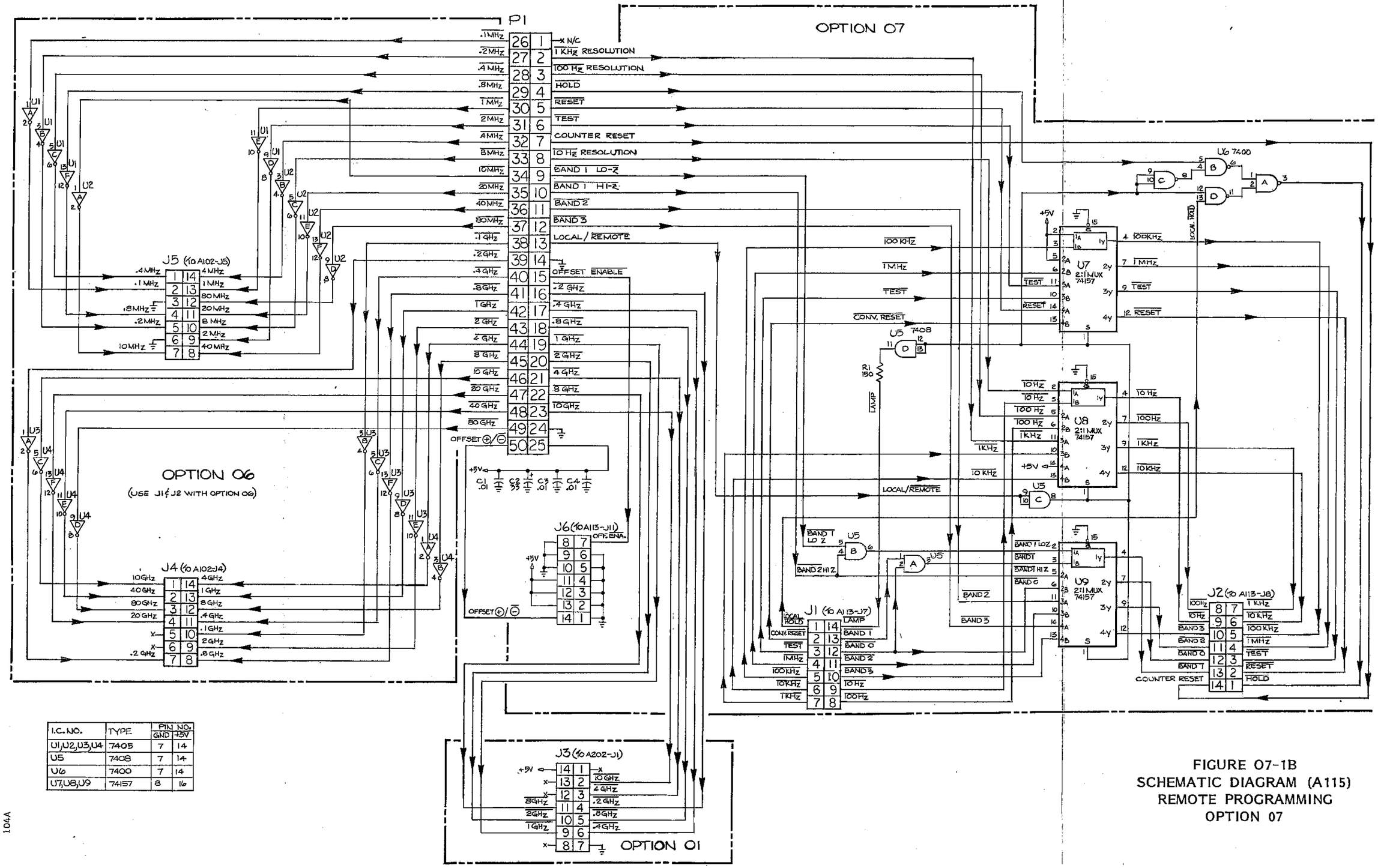
J3 Pin No.	Function
1	No Connection
2	1 kHz Resolution
3	100 Hz Resolution
4	$\overline{\text{Hold}}$
5	$\overline{\text{Reset}}$
6	$\overline{\text{Test}}$
7	Counter Reset
8	10 Hz Resolution
9	$\overline{\text{Band I, Lo-Z}}$
10	$\overline{\text{Band I, Hi-Z}}$
11	$\overline{\text{Band II}}$
12	$\overline{\text{Band III}}$
13	Local/$\overline{\text{Remote}}$
14	Ground

TABLE O7-1
J3 CONTACT GROUNDING FOR
REMOTE PROGRAMMING
OPTION 07



NOTE: COMPOSITE PCB ASSEMBLY FOR OPTIONS 01, 06, AND 07. ONLY A PORTION OF COMPONENTS SHOWN MAY BE USED ON ANY ONE OPTION.

FIGURE 07-1A
COMPONENT LOCATORS (A115)
REMOTE PROGRAMMING
OPTION 07



I.C. NO.	TYPE	PIN NO. GND	PIN NO. +5V
U1,U2,U3,U4	7405	7	14
U5	7408	7	14
U6	7400	7	14
U7,U8,U9	74157	8	16

FIGURE 07-1B
SCHEMATIC DIAGRAM (A115)
REMOTE PROGRAMMING
OPTION 07

104A

OPTION 09
BCD OUTPUT

09-1. DESCRIPTION

09-2. This assembly provides binary coded decimal outputs to the rear panel of the counter corresponding to the applied input frequency. A $\overline{\text{PRINT}}$ command indicates the presence of valid data, while an INHIBIT input is available to allow the user to prevent the information from being altered. Refer to Table 09-2 for rear panel connections.

09-3. Each output line from the latches associated with the counting chain (A102, A103) then feeds through an inverter to the rear panel Digital Output Connector J2.

09-4. A positive INHIBIT level (+2 to +50 V) turns on Q1. This in turn, generates a $\overline{\text{SEQUENCE INHIBIT}}$ command to prevent the counter from continuing its sequence. This command allows the user to prevent stored information from being altered.

BCD Code	1 - 2 - 4 - 8
Format	11 data digits in parallel form
"0" State Level	0 to 0.4 V, 5 mA current sink capability
"1" State Level	+5 V, 2kohm source impedance
Negative Ref	Ground
Positive Ref	+5 V, 22 ohm source impedance
Print Command	+5 V to 0 V step, fall time 1 microsecond 20 microsecond width. 2kohm source impedance.
Hold Off Requirement	Maximum: 50 V; minimum: 2 V.

TABLE 09-1
SPECIFICATIONS

Pin No.	Function	Pin No.	Function	Pin No.	Function
1	10^1 A	18	10^9 B	34	10^5 C
2	10^1 B	19	10^{10} A	35	10^5 D
3	10^2 A	20	10^{10} B	36	10^6 C
4	10^2 B	21	10^0 A	37	10^6 D
5	10^3 A	22	Inhibit	38	10^7 C
6	10^3 B	23	10^0 B	39	10^7 D
7	10^4 A	24	- Ref	40	10^8 C
8	10^4 B	25	+ Ref	41	10^8 D
9	10^5 A	26	10^1 C	42	10^9 C
10	10^5 B	27	10^1 D	43	10^9 D
11	10^6 A	28	10^2 C	44	10^{10} C
12	10^6 B	29	10^2 D	45	10^{10} D
13	10^7 A	30	10^3 C	46	10^0 C
14	10^7 B	31	10^3 D	47	10^0 D
15	10^8 A	32	10^4 C	48	Print Command
16	10^8 B	33	10^4 D	49	No Connection
17	10^9 A			50	Ground

NOTE: The 10^0 bit is the least significant digit, and corresponds to the 1 Hz output. A, B, C, and D, are the 1, 2, 4, and 8, bits of each binary coded decimal output digit.

TABLE O9-2
J2 CONTACT GROUNDING FOR
BCD DIGITAL OUTPUT
OPTION 09

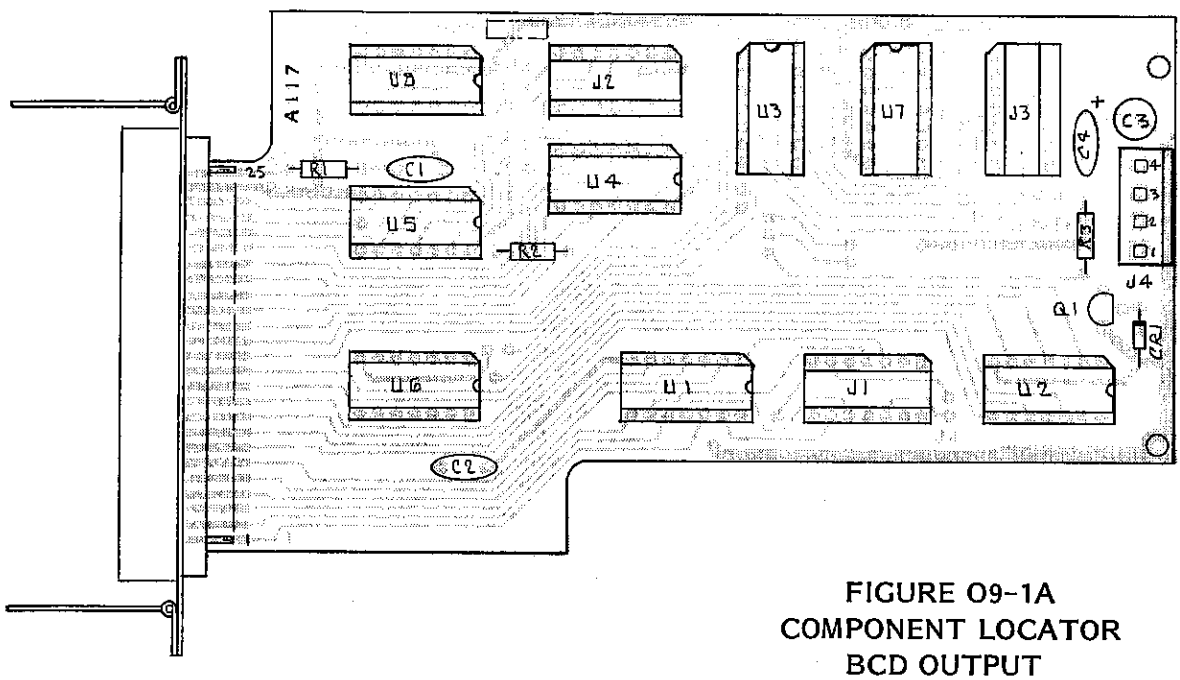
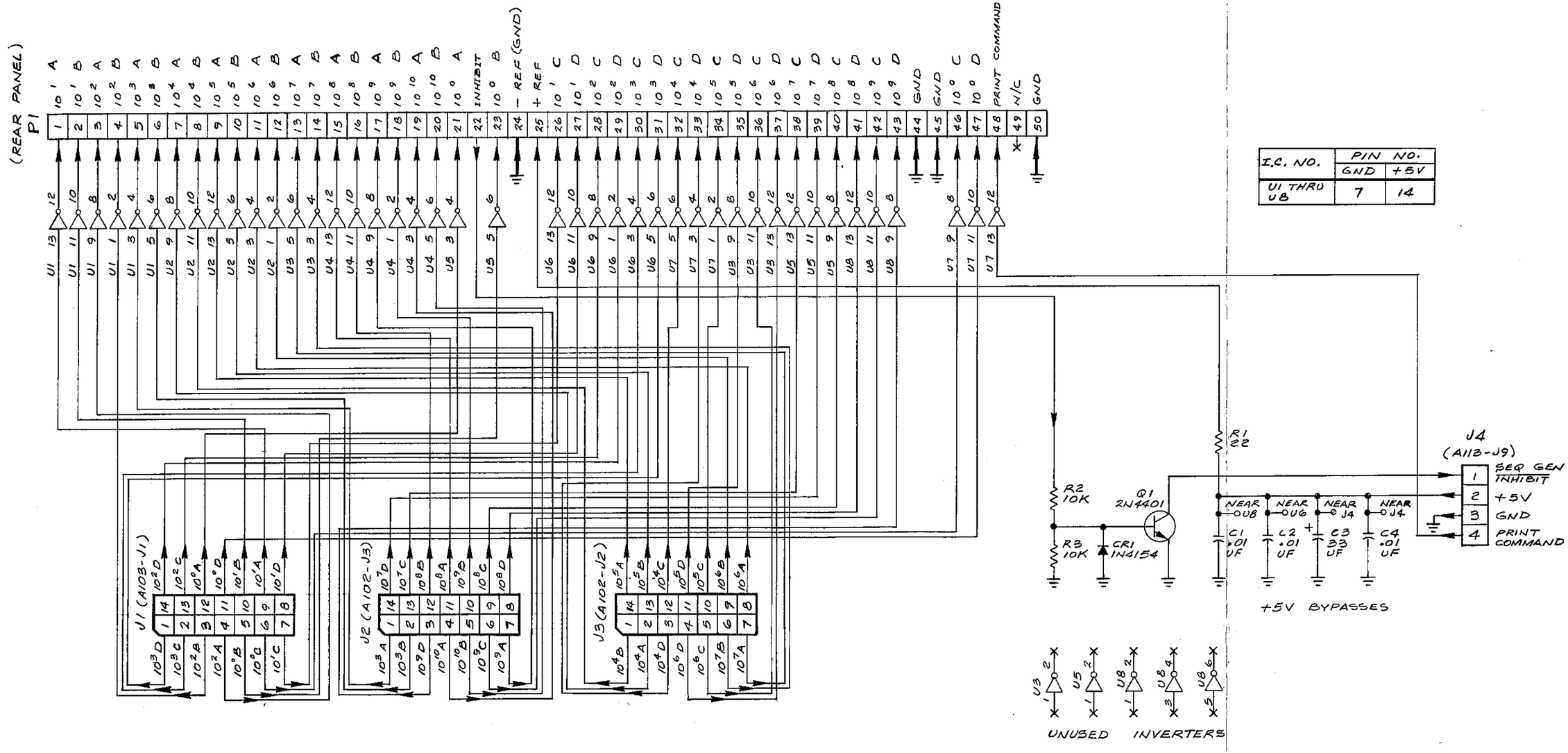


FIGURE O9-1A
COMPONENT LOCATOR
BCD OUTPUT
OPTION 09



I.C. NO.	PIN NO.	
	GND	+5V
U1 THRU U8	7	14

FIGURE 09-1B
SCHEMATIC DIAGRAM
BCD OUTPUT
OPTION 09

OPTION 10
REAR PANEL INPUTS

O10-1. DESCRIPTION

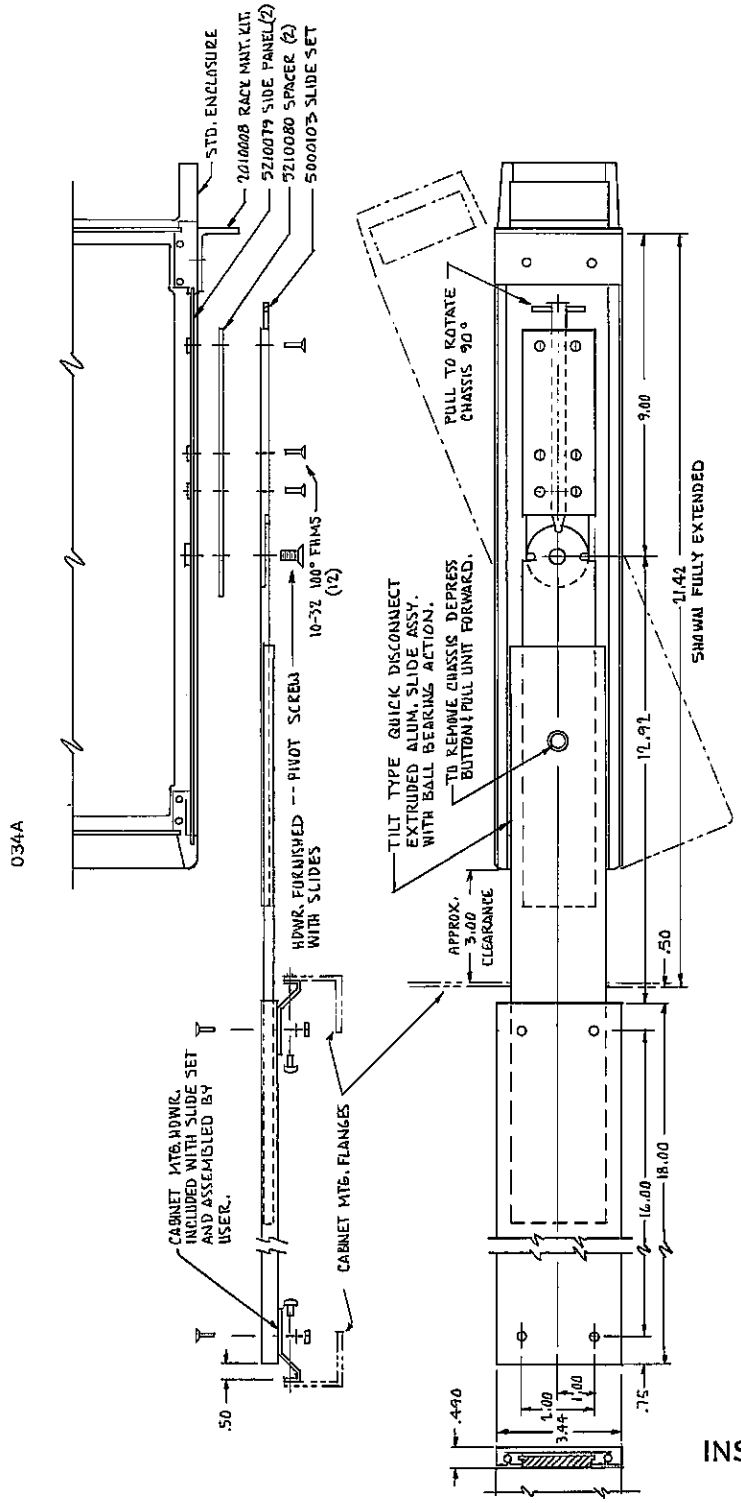
O10-2. Band I input connector and Preamplifier (A111), and Band II input connector, moved to rear panel. Converter assembly is reversed end-for-end, to place the Band III input connector at rear panel. All specifications remain as stated for front panel connectors.

OPTION 11
BAND II DELETED

O11-1. DESCRIPTION

O11-2. Band II input connector and Prescaler (A109) removed. Delete all manual references to Band II operation and components.

OPTION 13
RACK MOUNT/CHASSIS SLIDES



NOTES:

1. ALL MOUNTING HARDWARE AND HOLE SPACING CONFORMS TO MIL-STD-189.
2. TO INSTALL SLIDES IN FIELD: REMOVE TOP COVER AND TOP FRAME. MOUNT SPECIAL SIDE PANELS (P/N: 5210079) IN PLACE OF STANDARD PANELS.

FIGURE 013-1
INSTALLATION DIAGRAM
OPTION 13

EIP COUNTER REPAIR AND RETURN FORM

TO FACILITATE REPAIRS, PLEASE ANSWER ALL QUESTIONS AND RETURN THIS FORM WITH COUNTER TO: EIP INCORPORATED, 3230 SCOTT BOULEVARD, SANTA CLARA, CA 95051.

MODEL NO. _____ SERIAL NO. _____

1. Briefly describe trouble symptoms: _____

   _____

2. Check frequency range in which trouble occured:
   Band I 20 Hz-135 MHz _____ Band I 10-300 MHz _____ Band II _____ Band III _____

3. Would the counter show the correct display in the TEST position? Yes ____ No _____.

4. What was the approximate ambient temperature? _____ °F.

5. Did failure occur at turn on, or after some period of time? Turn on ____. After ____hours

6. At what frequency (ies) did counter fail to operate? _____.

7. What was the input power level at failure? _____ dBm (or mW).

8. Was the rear panel INT/EXT switch in the INT position? Yes _____ No _____.

9. What type of signal generator (or signal source) was being monitored by the counter at the time of failure? _____.

10. Please sketch (on the other side of this sheet), the test or operational set-up in use when the counter failed, and any additional comments regarding this instrument.

11. In the event counter repair cost is not covered under the EIP standard warranty, please complete the following:

    a. Maximum allowable charge without further customer approval: $ _____.

    b. P.O. No. _____ Date _____ Buyer _____.

    c. Billing address: _____

    _____.

12. Name of person making this report (PLEASE PRINT): _____.

    Your phone number: (Area Code: _____) _____ Ext: _____.

CUSTOMER INFORMATION	SHIPPING INFORMATION
OWNER _____	SHIP TO _____
ADDRESS _____	ADDRESS _____
CITY _____	CITY _____
STATE _____ ZIP _____	STATE _____ ZIP _____
COUNTRY _____	COUNTRY _____

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